FPGA - Overview of JPL Efforts under NEPP

Dr. Douglas Sheldon
Jet Propulsion Laboratory
California Institute of Technology

Overview

- Introduction
- Technology
- Radiation
- Packaging
- Applications
- Software
- Future

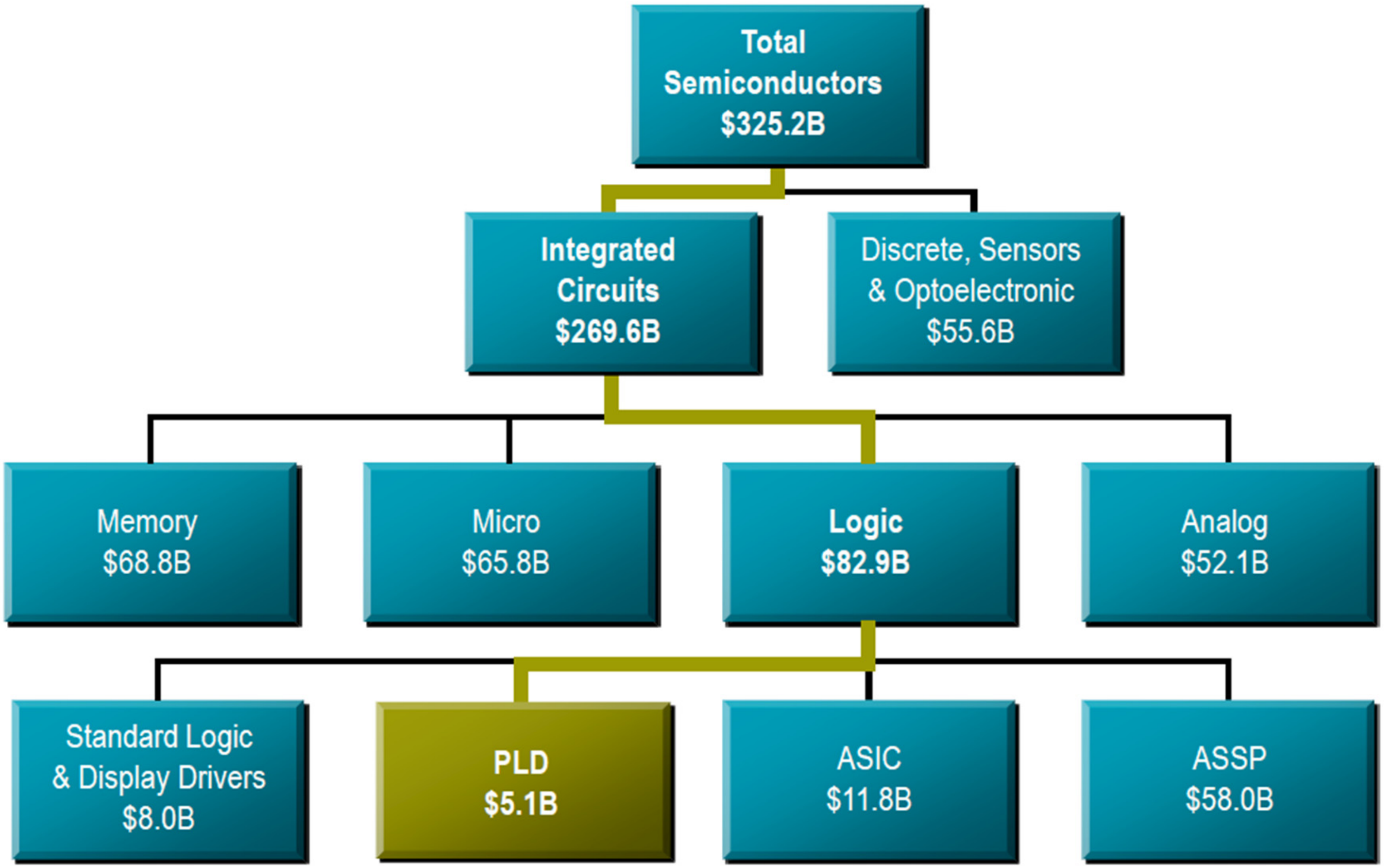
Introduction

- JPL/NEPP FPGA efforts are focused on:
  - Technology qualification
  - Risk management
  - Packaging qualification and development
  - Guideline development
  - Agency wide support for community development

FPGAs at NASA

- FPGAs represent the main VLSI technology driving force for all NASA missions.
- All current generation and future generation spacecraft will have literally dozens of FPGAs on board doing a wide variety of tasks.
  - MSL – 60+ FPGAs
    - Bus control, telemetry, encoders, telecom, NVM, algorithm
- Concerns/opportunities:
  - New materials qualification and reliability
  - Power management
  - High bandwidth communication related issues
  - Single event/soft error mitigation schemes
  - Programming vulnerabilities

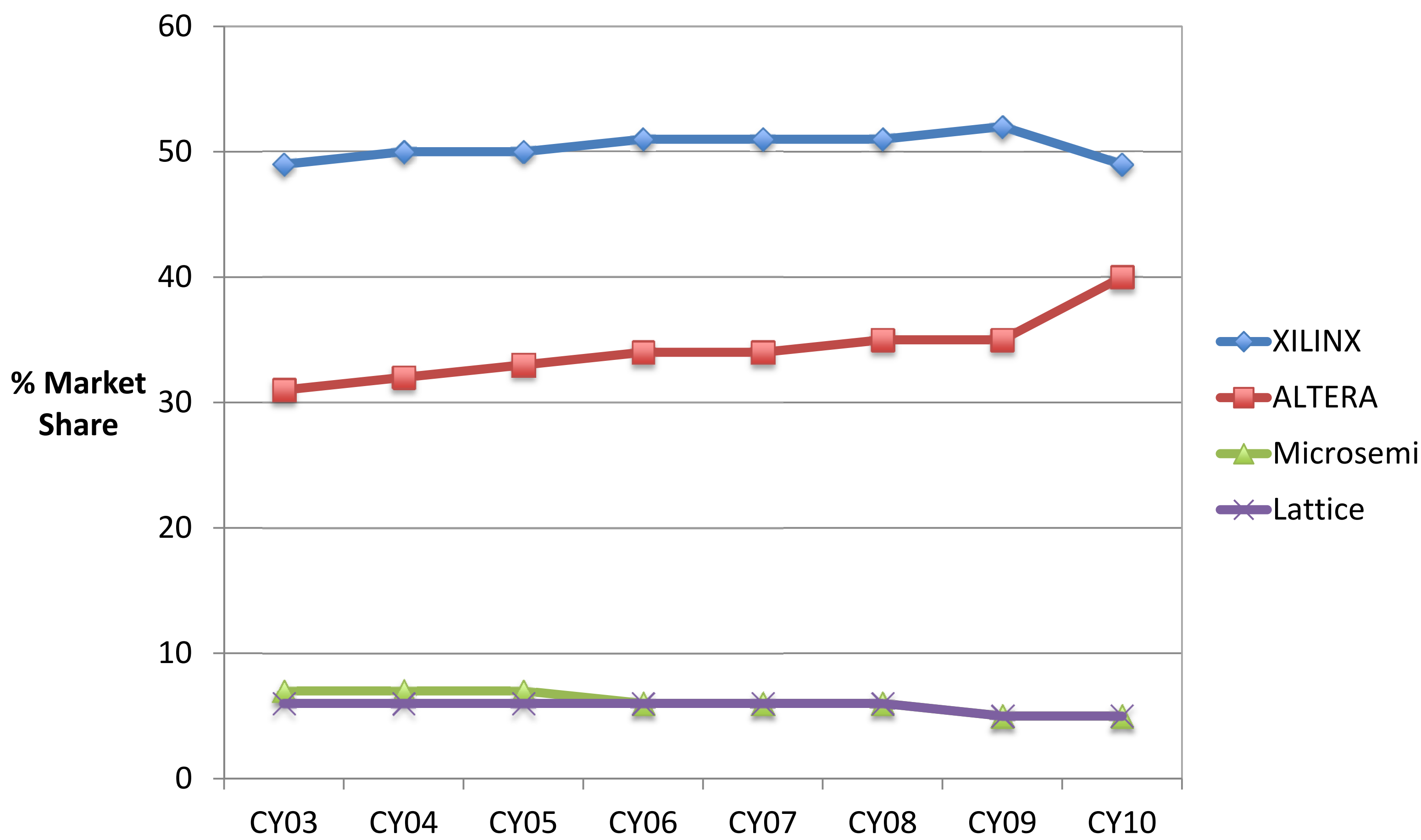
Worldwide Semiconductor Market 2011



Source: iSuppli, March 2011

PLD = Programmable Logic Devices/FPGAs

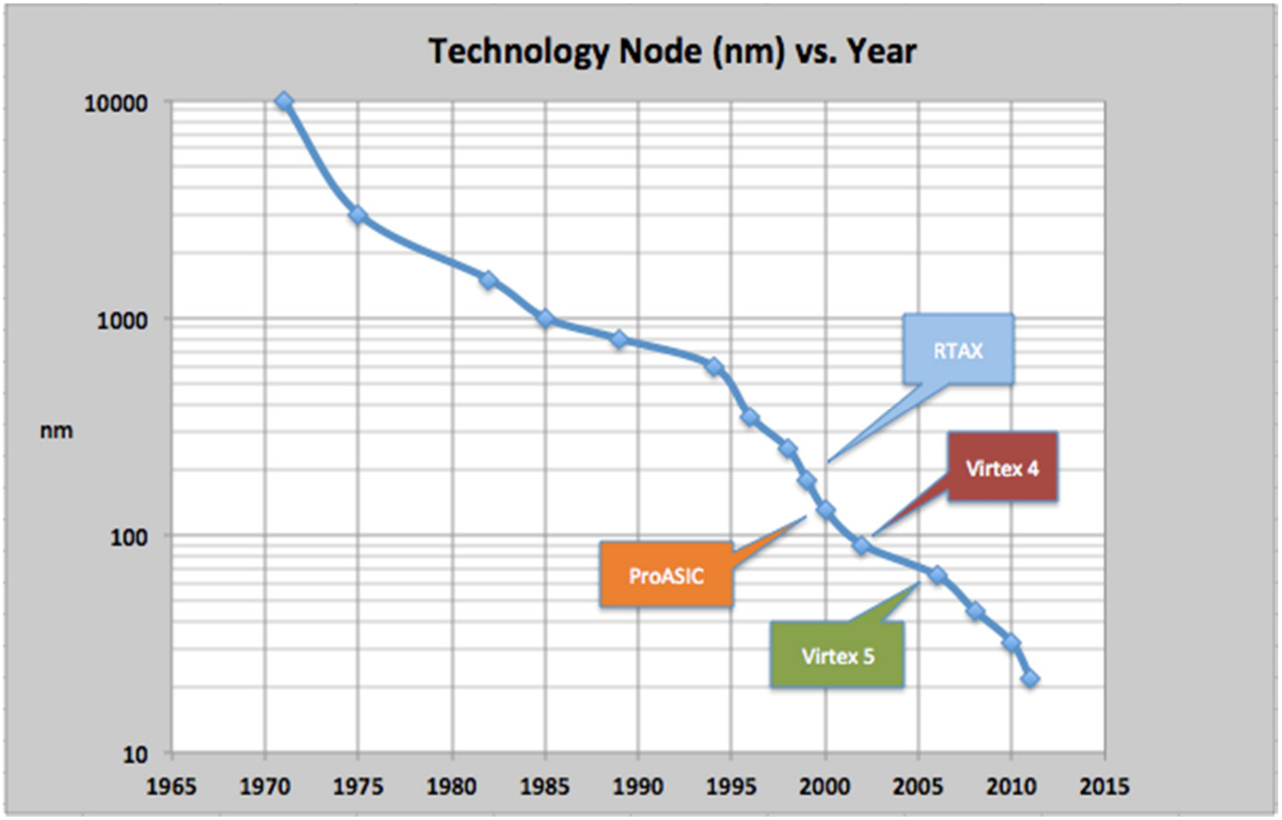
PLD Market Share



iSuppli

Technology

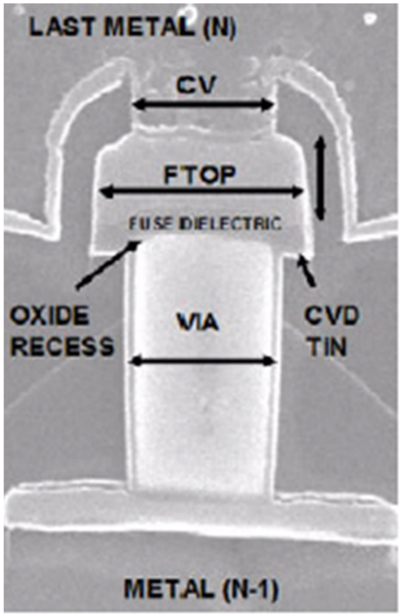
Technology Node vs. Year of Introduction

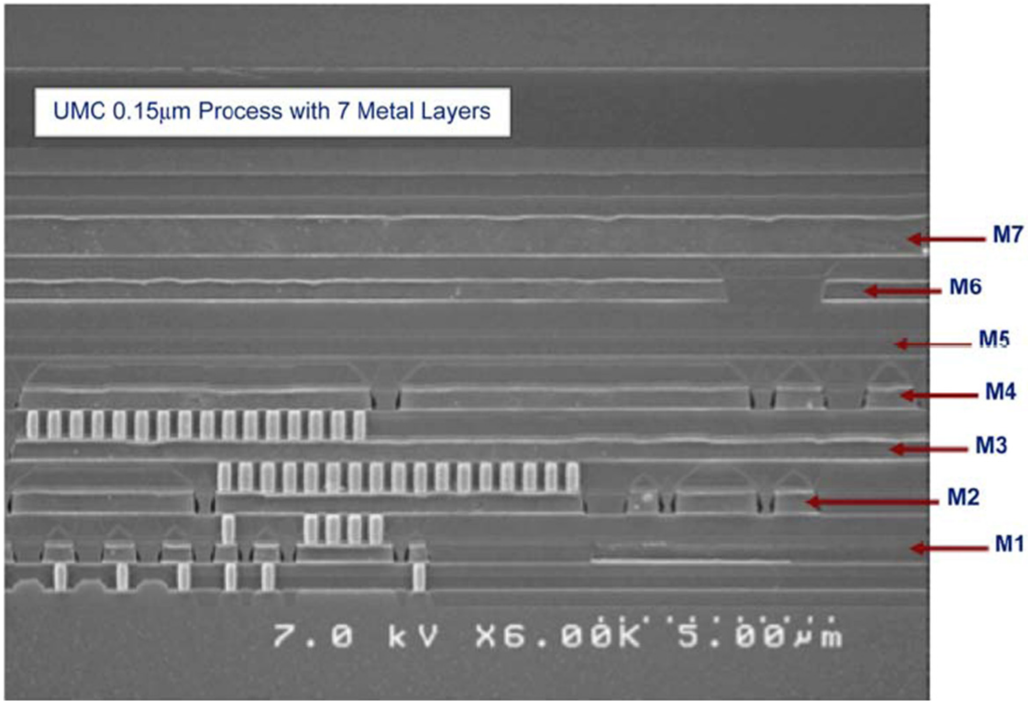


- Space users are many generations behind in FPGA technology
- New technology issues for space community are 'old' for commerical community

Space FPGA Technology

- Currently RTAX is latest generation in flight
  - 150nm/7 layer AlCu:TiN/~3nm tox/antifuse
  - Custom designs for life test/burn evaluation and antifuse qualification





Actel-RTAX-S Testing and Reliability Update, 2007

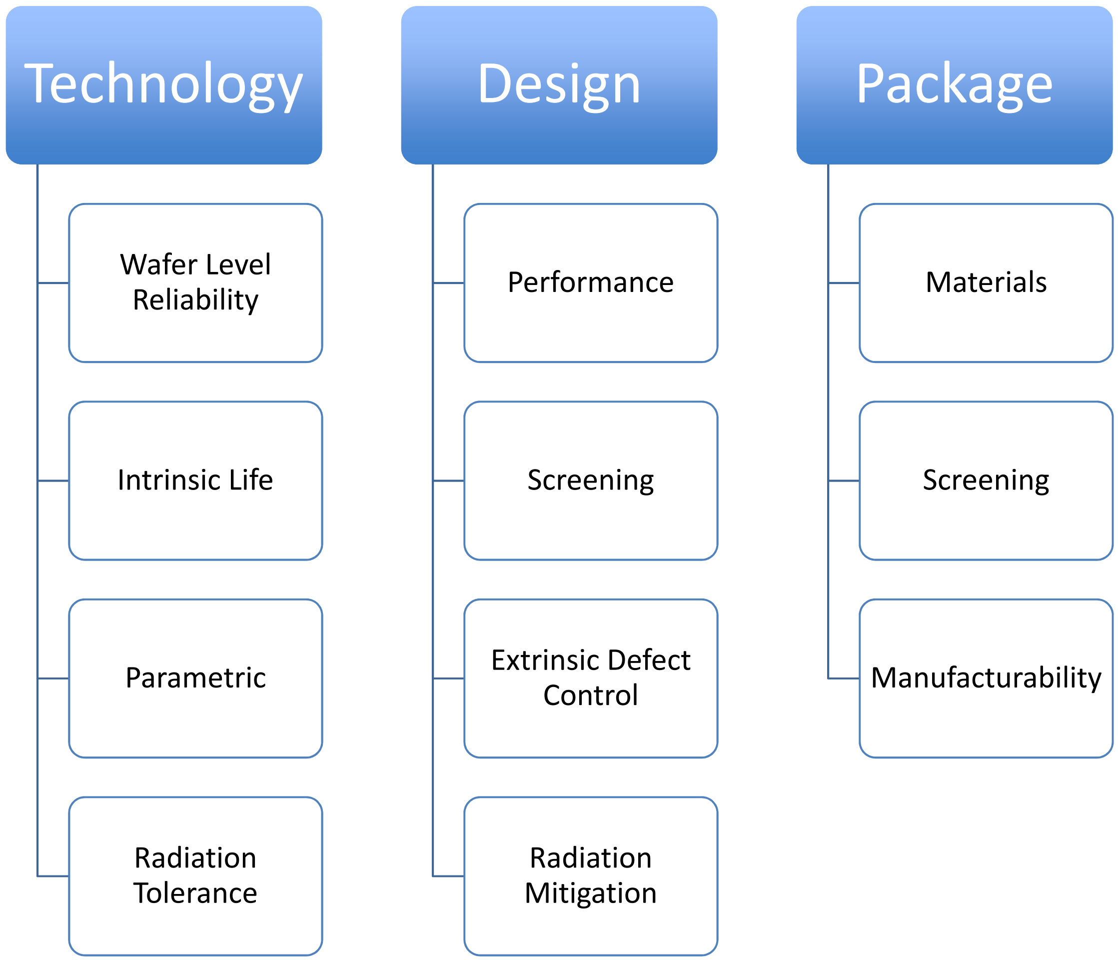
What’s next for Space FPGA Technology?

Technology node	Name	Type
130nm	RTP3	Flash
90nm	Virtex 4	SRAM
65nm	Virtex 5	SRAM
65nm	RTP4	Flash

- Use of flash and 90nm and below technologies introduce significant new qualification and reliability issues.
- What’s the methodology to do this…?

FPGA Technology Qualification Methodology

Three main areas for emphasis



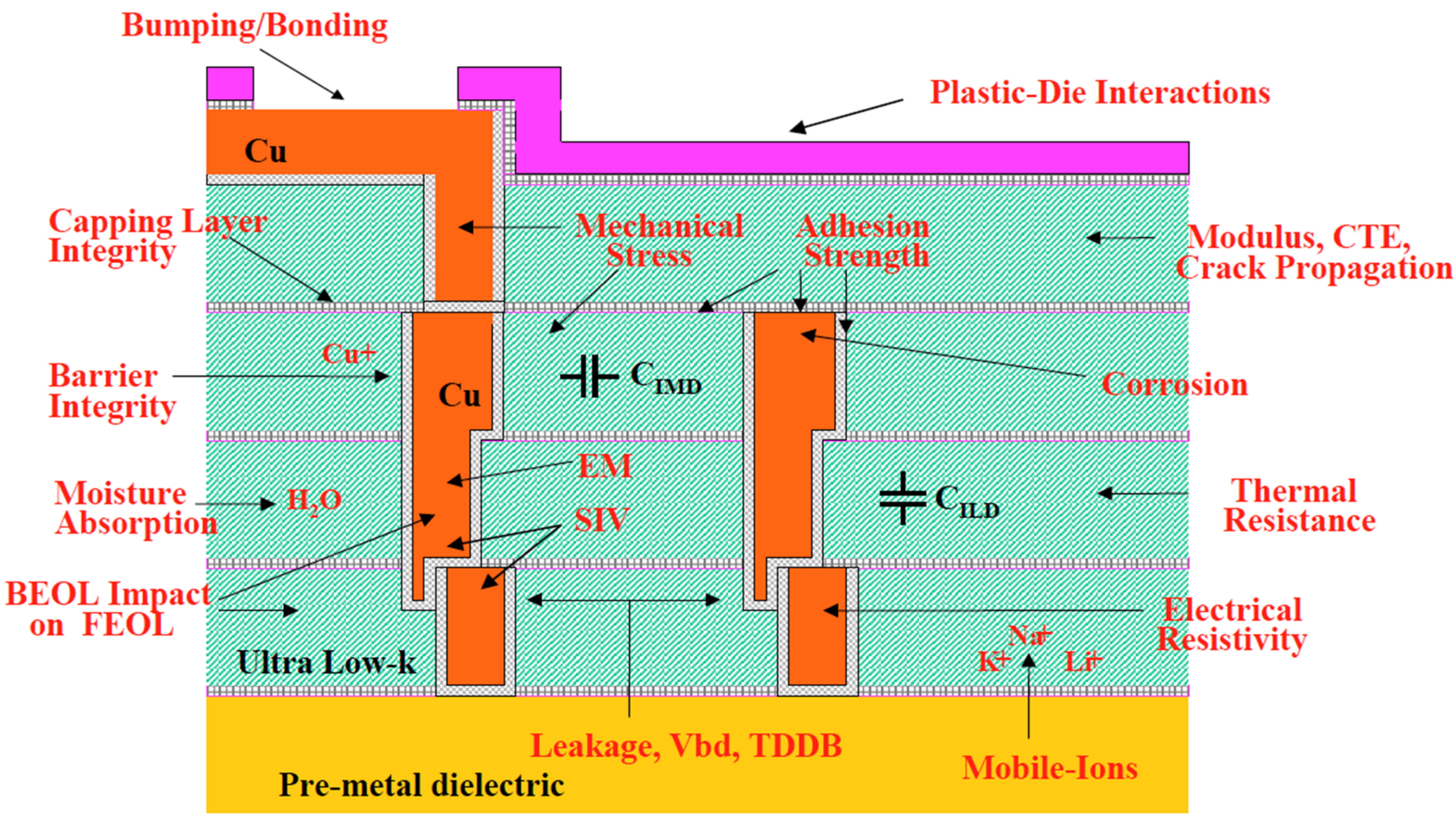
FPGA Technology Qualification Methodology

- Fabless FPGA companies and wafer fabs have a unique relationship for technology qualification*.
- Each has responsibilities and both must share at the same time.
- Space community is additional partner in the qualification relationship.
  - *We can't do most of these tasks, yet we must understand them and influence them where we need to.*

	Infant Mortality - Extrinsic Failures	Long Term Life - Intrinsic Failures
Wafer Fab	• Defect Reduction • Excursion Prevention • Outlier elimination	• Wear out data/models • WLR testing • Process standardization
Joint Fab-Fabless	• Wafer parametric limits • Yield acceptance limits	• Wafer failure criterion • Process customization
Fabless Design	• Defect Isolation • Product level screening/BI	• Use conditions & wear out rules • Design for reliability • Product reliability characterization
Space community	• *Custom BI/screening* • *Custom designs for reliability/radiation evaluation*	• *Derating* • *Mission specific requirements* • *Additional reliability/radiation testing*

*S. Y. Pai, 'Reliability Framework in a Fabless-Foundry Environment", IRPS 2009

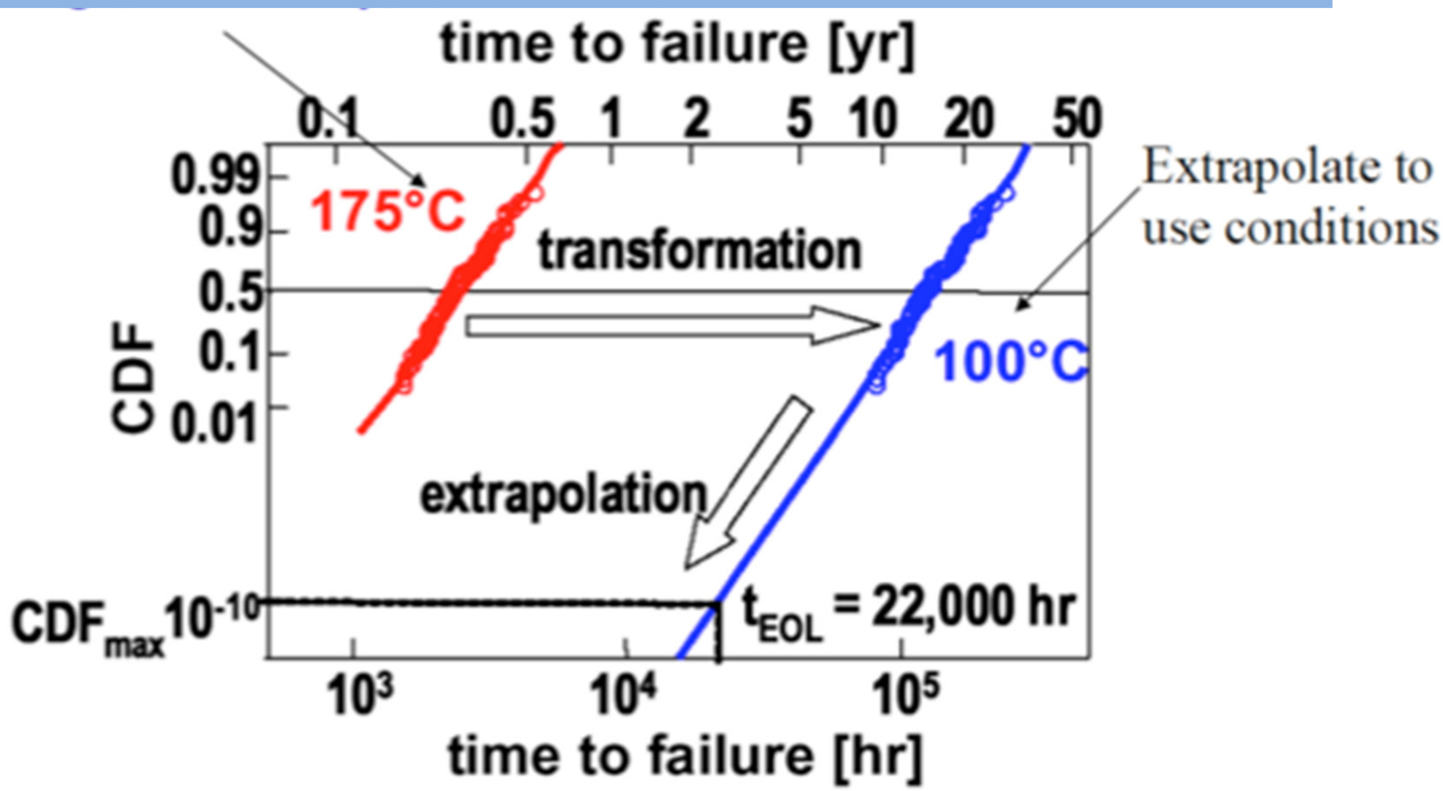
FPGA Technology Reliability Issues



http://stanford-online.stanford.edu/sesi04moore/docs/LowKDielectics4.pdf

Accelerated Life Test

Accelerate fails with temperature, current, voltage and/or humidity to reduce test time

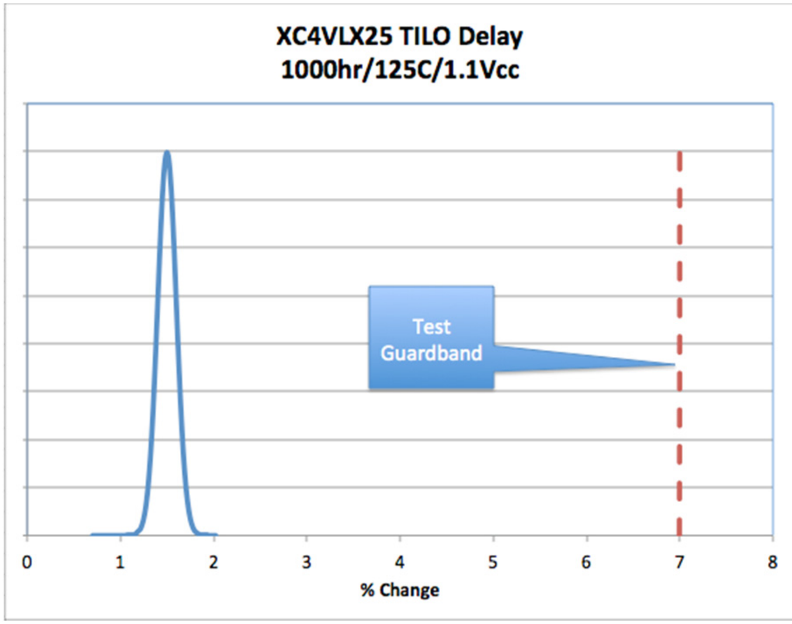


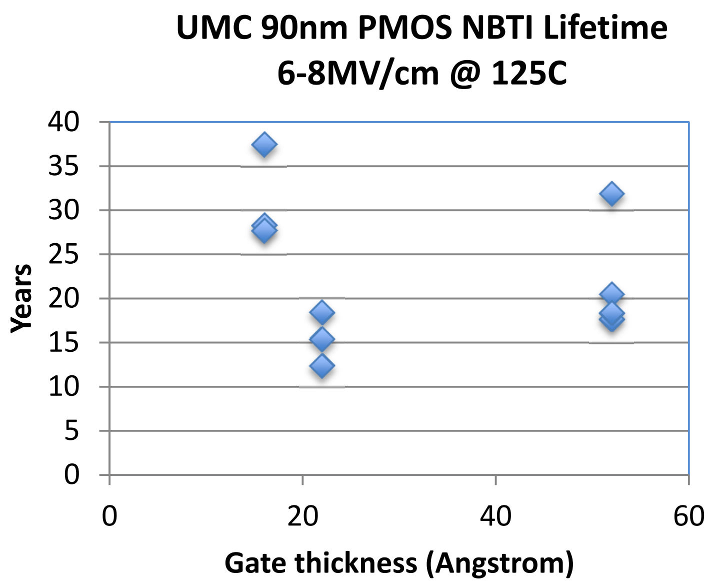
A. Fischer et al., Int. Rel. Phys. Symp. Proc., 2001, p. 334.

Example 90nm Technology Qualification Data

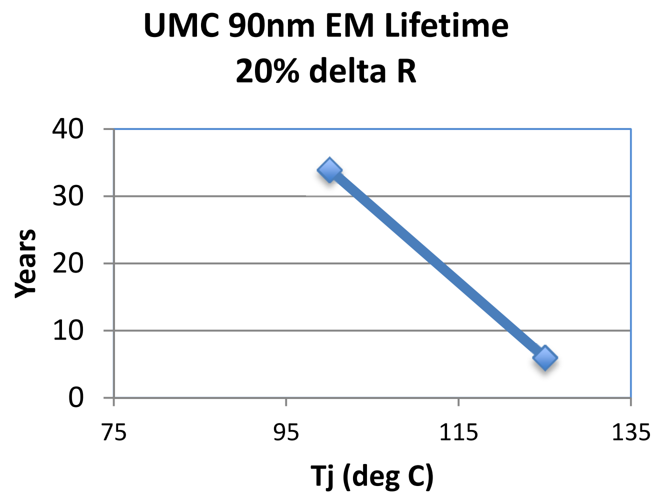
Technology qualification highlights:

- Lot requirements
- Derating
- Mission definition of failure
- Test structures and analysis





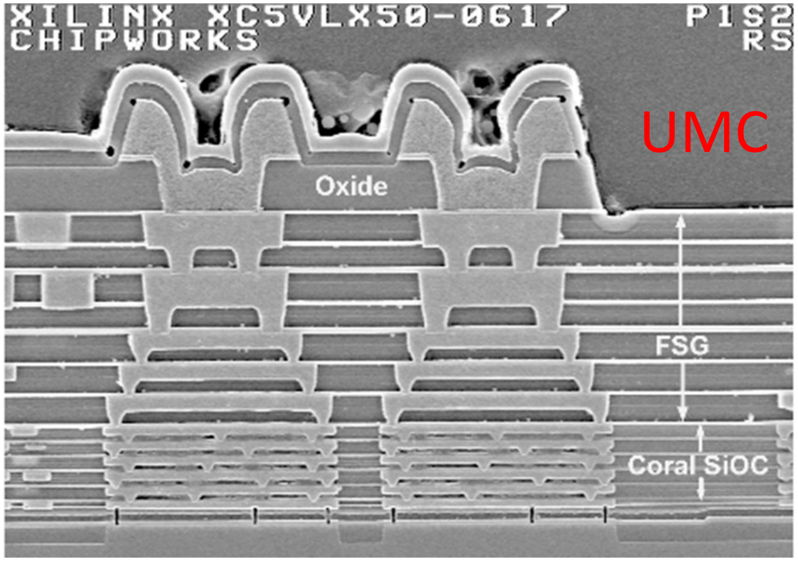
Notice lot variation

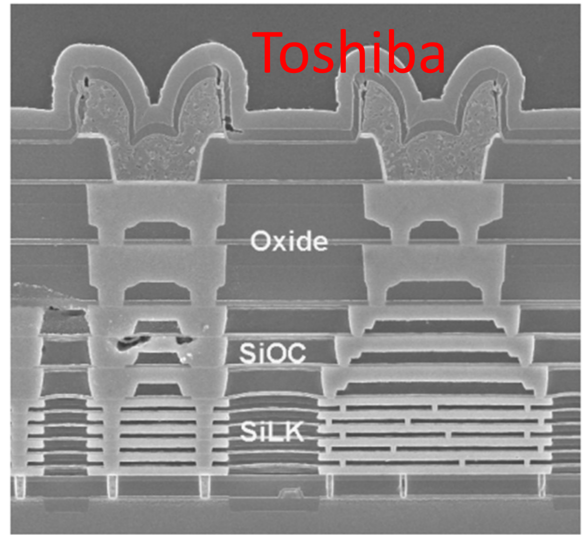


<10yrs life at high Tj

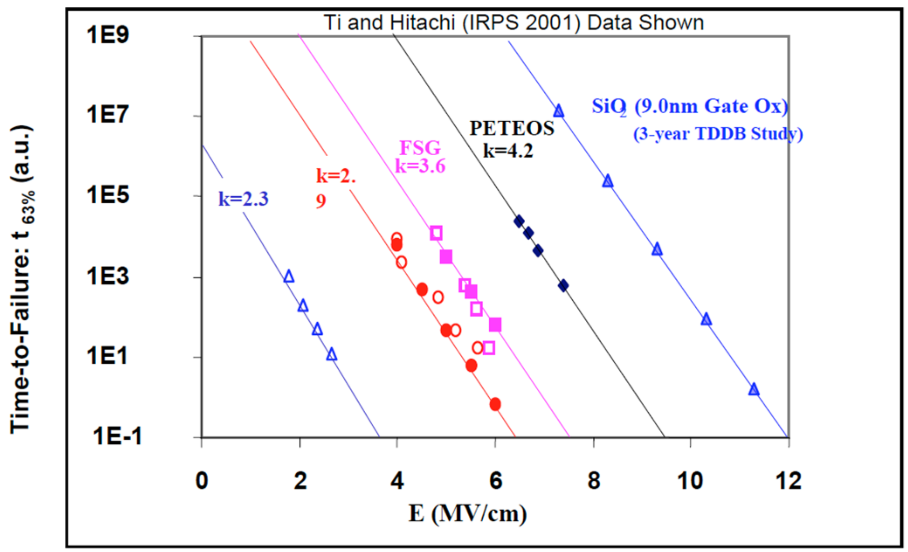
"Virtex-4, Aerospace and Defense UMC-12A 90 nm" - Xilinx

Foundry Differences – Virtex 5
Intermetal Dielectric Differences





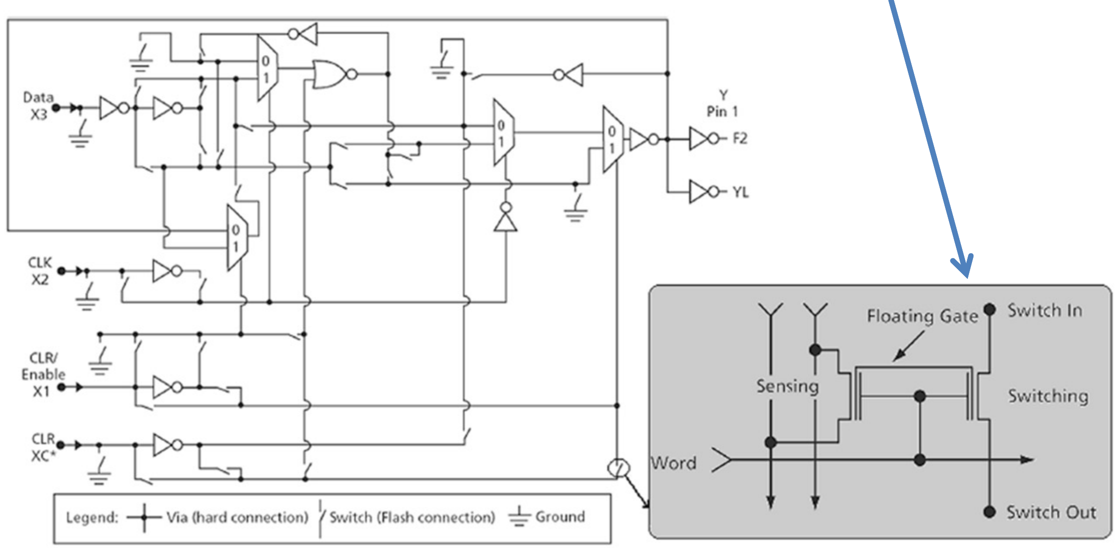
- CVD vs. Spin-On ILD/ UMC vs. Toshiba
- UMC - CVD carbon-doped oxide (SiOC) in M1-M6
- Toshiba - SiLK is used at the M1 – M6 levels
- SiLk k~2.65 vs. CVD k~2.8-3.0
- Subtle foundry differences can have possible significant impact on long duration, high reliability missions – particularly packaging

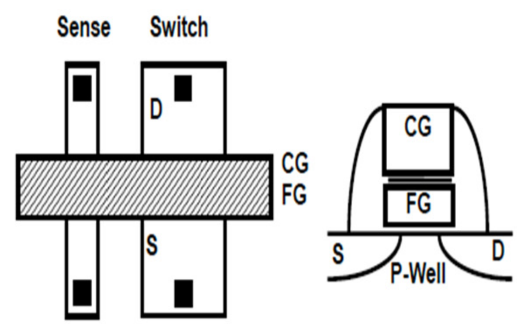


http://www.chipworks.com/en/technical-competitive-analysis/resources/technology-blog/2006/11/more-on-the-virtex-5/

Flash Based FPGA

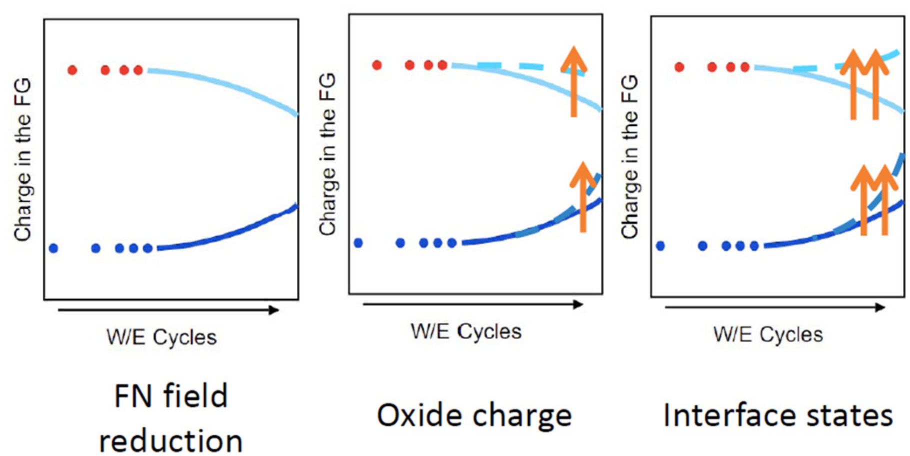
- Non-volatile and reprogrammable/Low power/Rad tolerant
- Flash based interconnection is new to space applications
- Two transistor (2-T) cell with common floating gate between two devices
- The “Switch” device is used as the configuration switch in the FPGA fabric.
- The “Sense” device is used to program the cell as well as for sensing the threshold voltage of the switch.

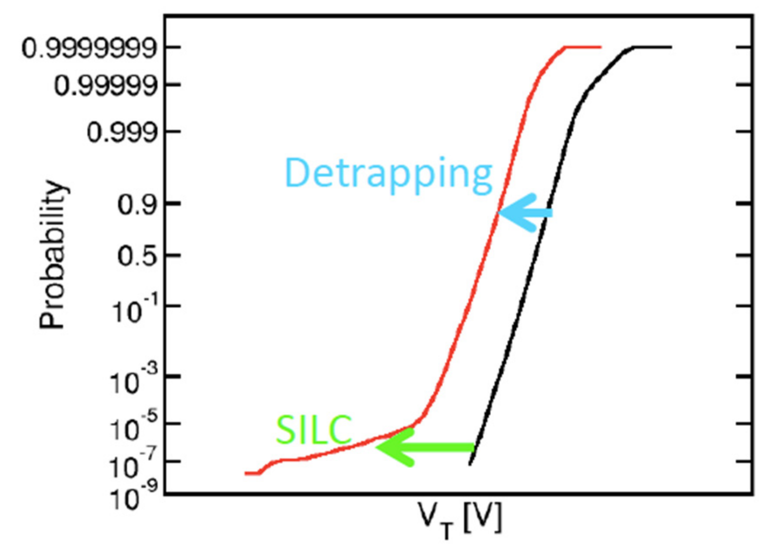




Flash FPGA Technology Qualification

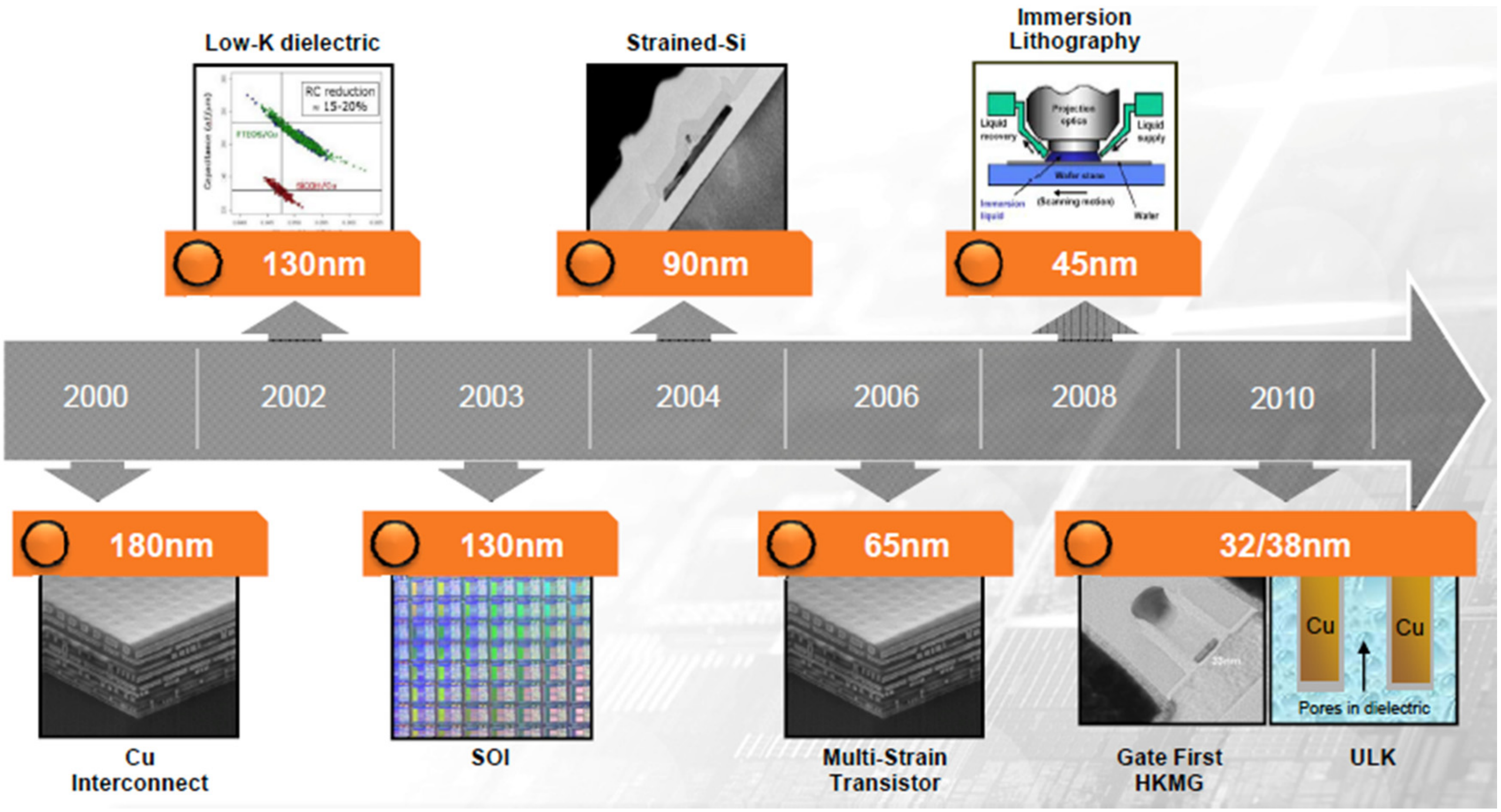
- Flash cell reliability driven by electric field and temperature.
- Flash devices have data retention and endurance as new failure mechanisms that need to be included into overall FPGA qualification plan.
  - 50% P/E cycle limit + 1,000 HTOL?
  - Flash memory devices require error correction and wear leveling to ensure reliability as densities have scaled. Same concerns here?
  - Temperature dependence of program/erase operation?
  - The behavior of individual bits can dominate reliability.





Flash Memory Reliability IRPS 2009 A. S. Spinelli and C. Monzio Compagnoni

New Technology Development Issues are just getting started



- FPGAs are now technology drivers for top tier commercial foundries.
- We have many exciting new technologies to look forward to!

Recent Radiation Results
FPGA Technology

Greg Allen - JPL

Introduction

- Historically, reconfigurable FPGAs have had relatively sensitive radiation responses
  - Altera (SEL)
  - Actel (TID/SEU)
  - Xilinx (SEU/SEFI)
- The aerospace community has traditionally used one time programmable FPGAs (e.g. antifuse) due to relative SEE/TID robustness
  - Increasing interest in recent years to implement reconfigurable devices (Xilinx QR in particular)
  - Lead to challenges in mitigation, verification, and system error rate calculations

Goals

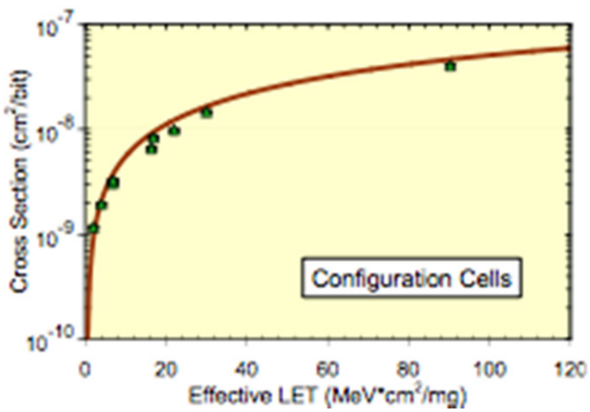
- Full static radiation characterization of the Xilinx XQR5VFX130 SIRF device in conjunction with the Xilinx Radiation Test Consortium
  - Provide a methodology for NASA missions to determine error rates and mitigation methodologies (as necessary)
- Evaluate other reconfigurable FPGA vendors for SEE/TID
  - SiliconBlue iCE65
  - Altera Stratix IV/Stratix V
- Evaluate non-volatile memory products as available
  - SONOS devices
  - Mitigated flash

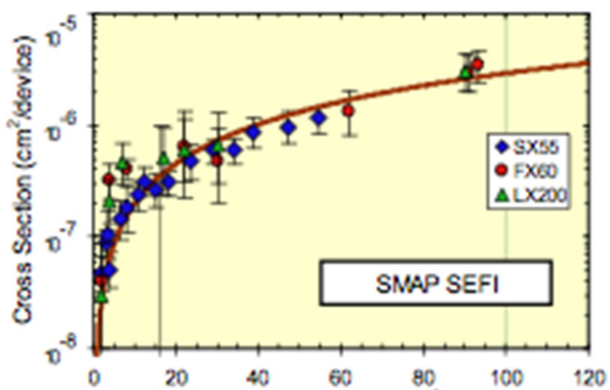
SEE Mitigation—TMR and RHBD

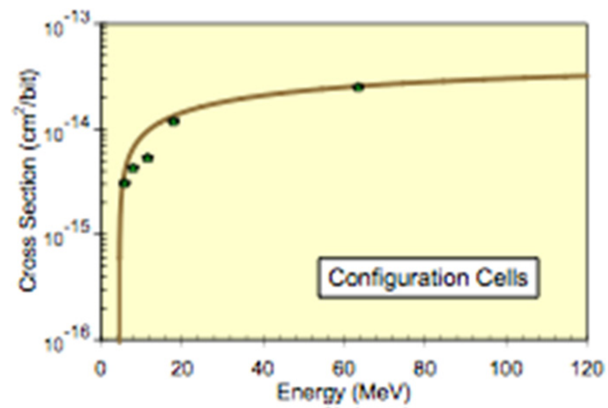
- EDAC (Virtex-4)
  - TMR and scrubbing
    - Complicated implementation
    - Increased engineering cost
    - Complicated verification and error rate calculation
- RHBD (Virtex-5)
  - Transparent implementation from the designer perspective
  - Complex radiation response requires new flight qualification methodologies

General FPGA Radiation Effects Evaluation Path

- Single-Event Latchup
- Static Characterization (Heavy Ion/Proton)
  - Configuration Elements, RAM, Registers, and Device-Level Single-Event Functional Interrupt
- Total Ionizing Dose Susceptibility
- IP Block Characterization (Dynamic Testing)
  - Clock Management, I/O, Processors, Multipliers, etc.







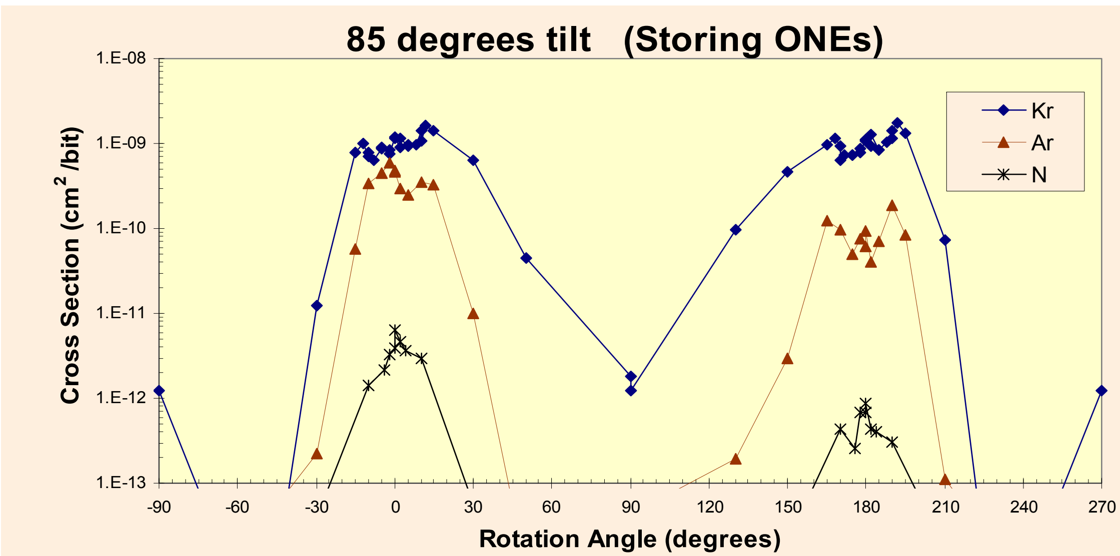
Moving from Virtex-II/Virtex-4 SEE Verification to Virtex-5

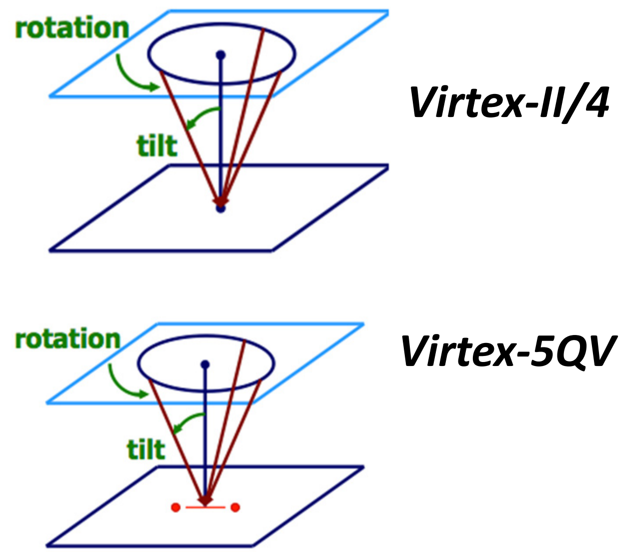
- Previous Virtex devices' error rate was dominated by static elements (namely configuration and BRAM cells).
- A general outline for developing a mitigation scheme is outlined below:
  - What is the underlying, unmitigated system error rate?
    - **Fault injection, accelerator testing, or software estimation**
  - What is the probability of observing an error?
    - **Error rate and operating period**
  - What is the level of mitigation that is going to be required?
    - **Engineering vs. reliability**
  - What level of configuration correction is going to be required?
    - **Level of error persistence**
  - How will this mitigation scheme be verified?
    - **Fault injection or accelerator testing**

Enabling, yet SEU sensitive devices, require complex upset mitigation to use in most cases

Moving from Virtex-II/Virtex-4 SEE Verification to Virtex-5

- Virtex-5 RHBD has virtually removed the static elements from the error model. Now dominated by SETs.



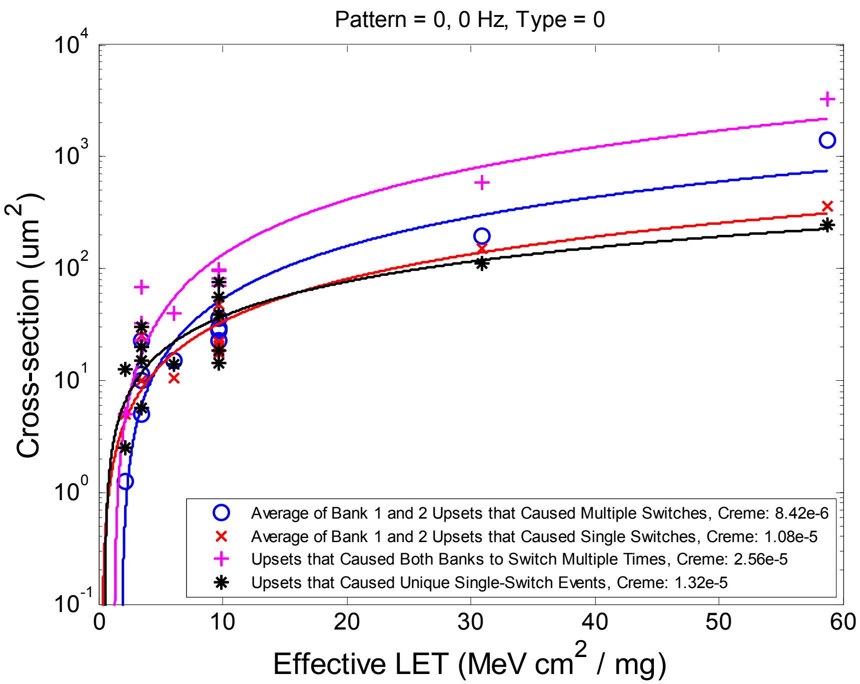


New methodology developed for characterizing dual-node configuration cells. The focus is now shifted to embedded IP elements.

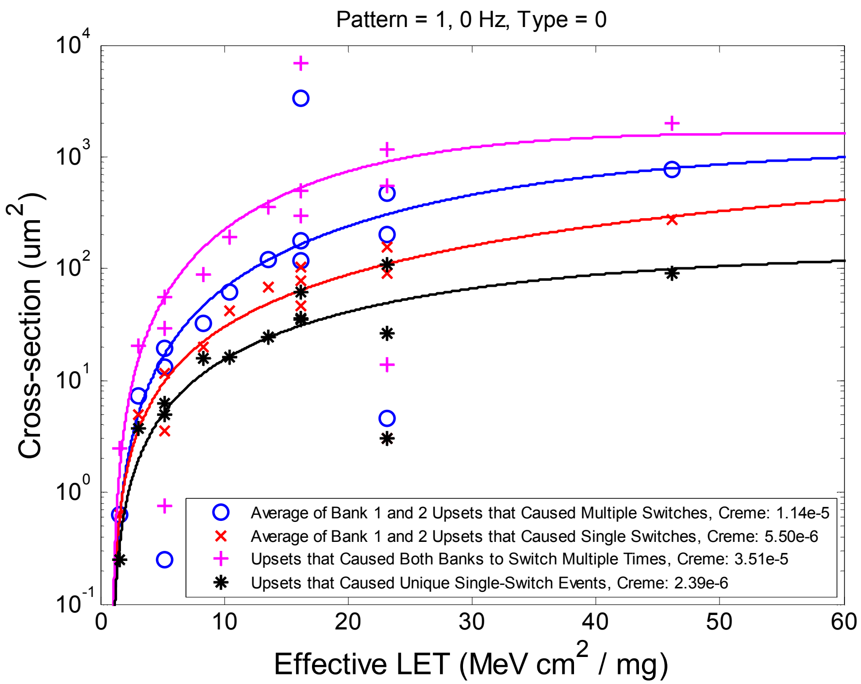
Technical Highlights

- CMT testing almost completed

DCM

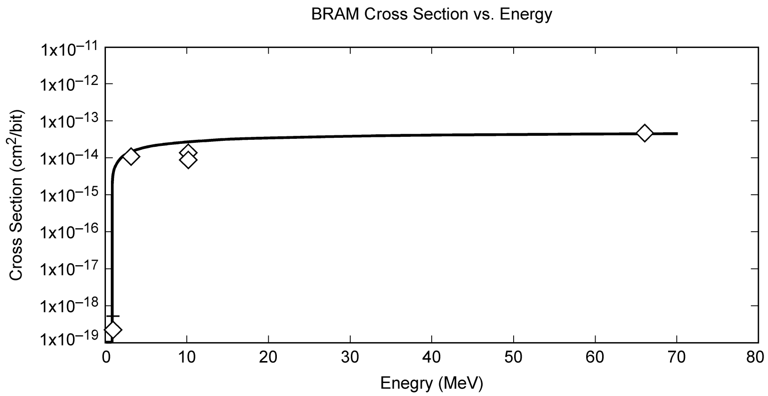


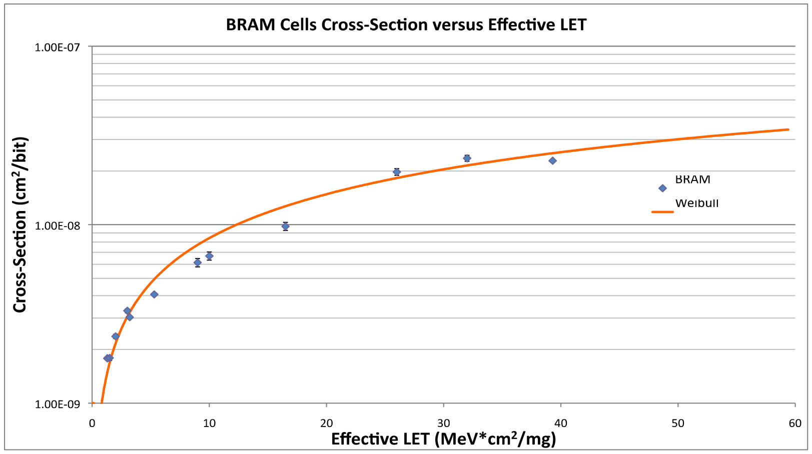
PLL

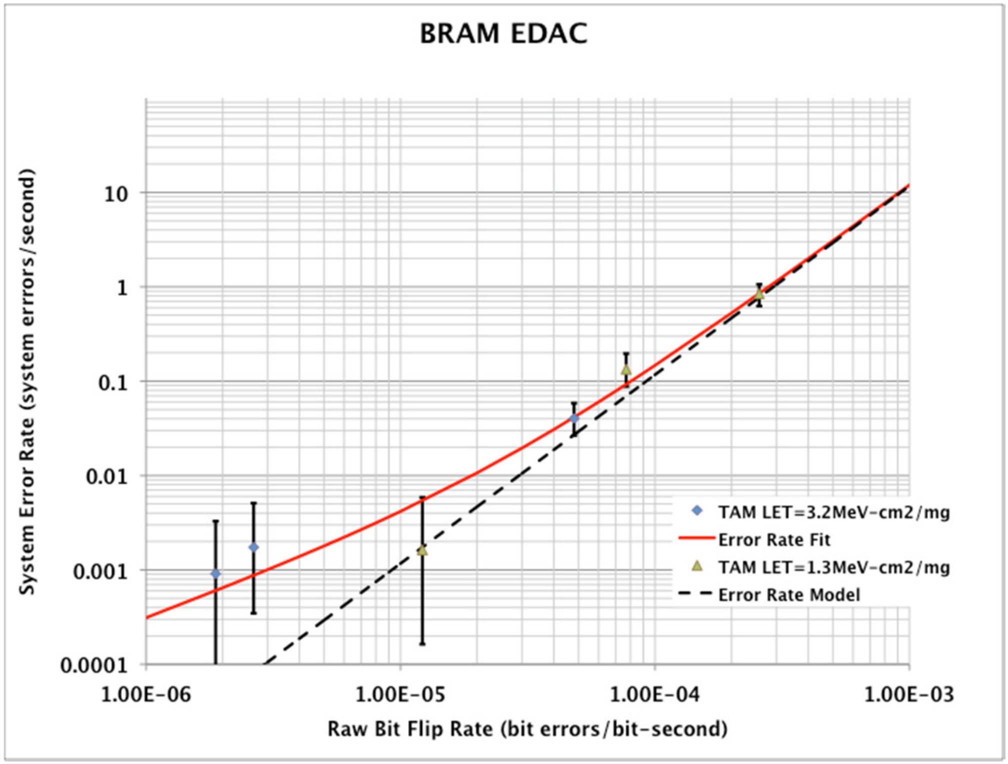


Technical Highlights

- BRAM and embedded BRAM EDAC evaluated for SEE

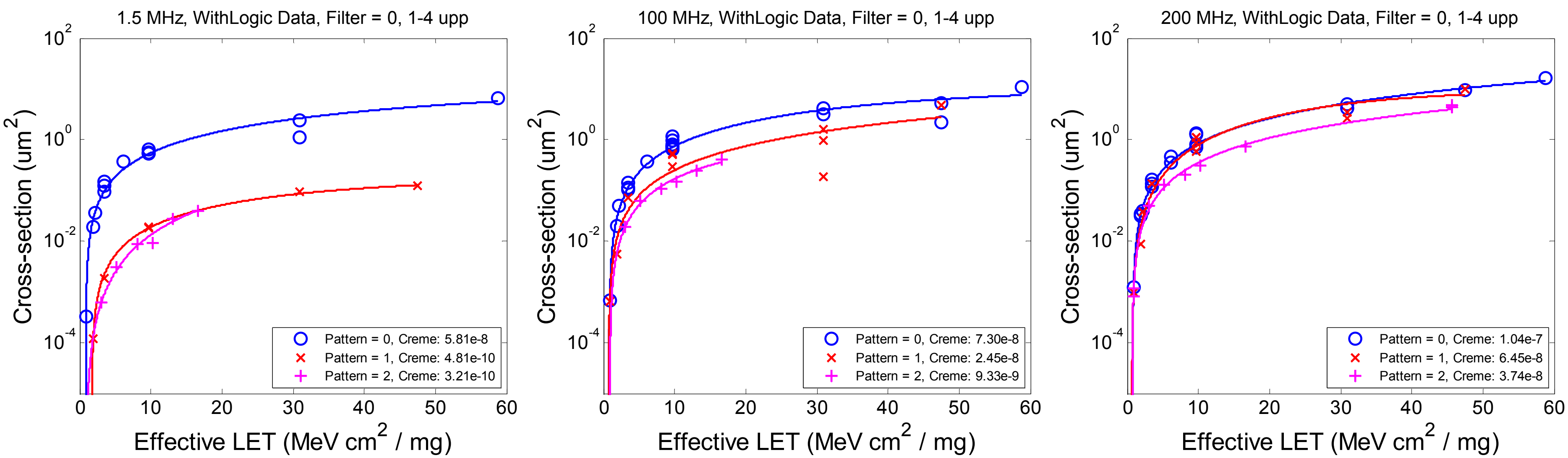






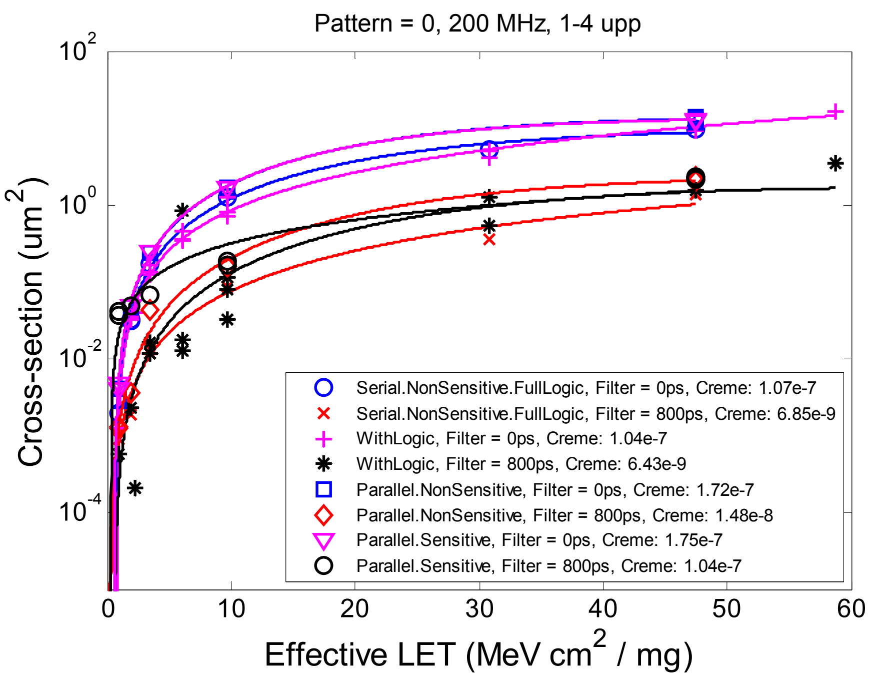
Technical Highlights

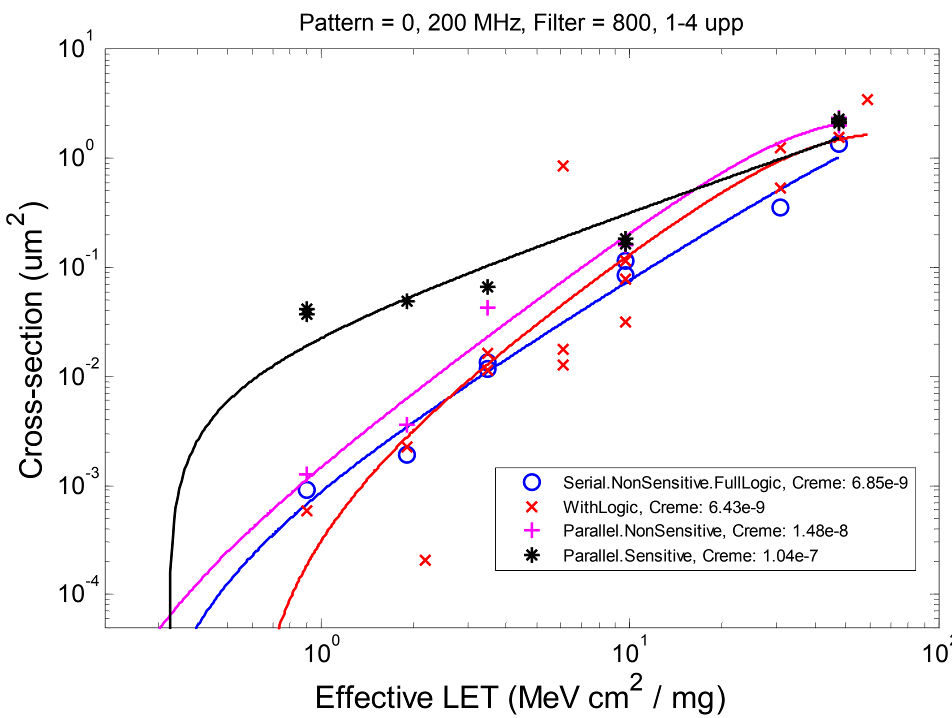
- SET testing on CLB
  - Frequency dependence evaluation



Technical Highlights

- SET testing on CLB
  - SET Filter and Logic configuration (parallel vs. serial)





Going Forward

- System fault characterization methodology for XQR5VX130
  - Accelerator testing of SEFIs is complicated: cross-section dependence on LET, flux, rotation/tilt, and configuration monitor implementation
  - System-level qualification is convoluted:
    - Beam testing won't express error rate from configuration bit upsets
  - FY11 Product will be a complete XQR5VFX130 static/pseudo-static characterization report
  - FY12 Product will be recommendations to estimate system error rates for various XQR5VFX130 designs.
- Unhardened IP characterization qualification
- Continued SEE testing of SiliconBlue and Altera FPGA

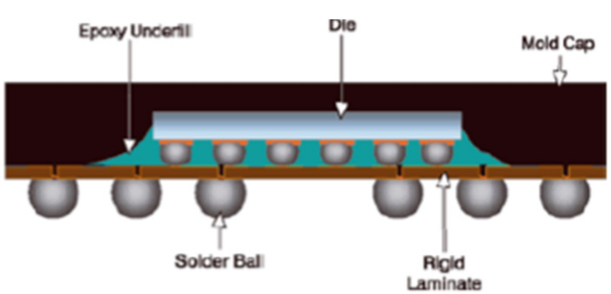
Complex SEE response will require flight qualification guidelines to be updated for this device

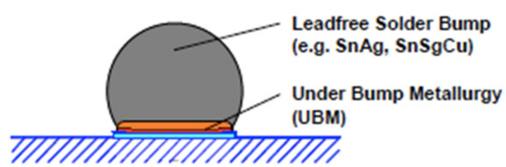
Packaging

FPGA Packaging

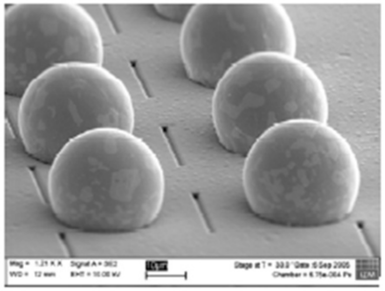
- The non-hermetic package is the beginning of a new era in packaging technology qualification - High density, high power VLSI devices
- Important implications for space applications
- What is required for risk management?

- Failure classification standards
- Identification of failure mechanisms
- Improved failure analysis techniques
- Electrical/thermal/mechanical simulation
- Lifetime models with defined acceleration factor
- Test vehicles for specific reliability characterization
- Early warning structures
- Space Quality Manufacturing guidelines



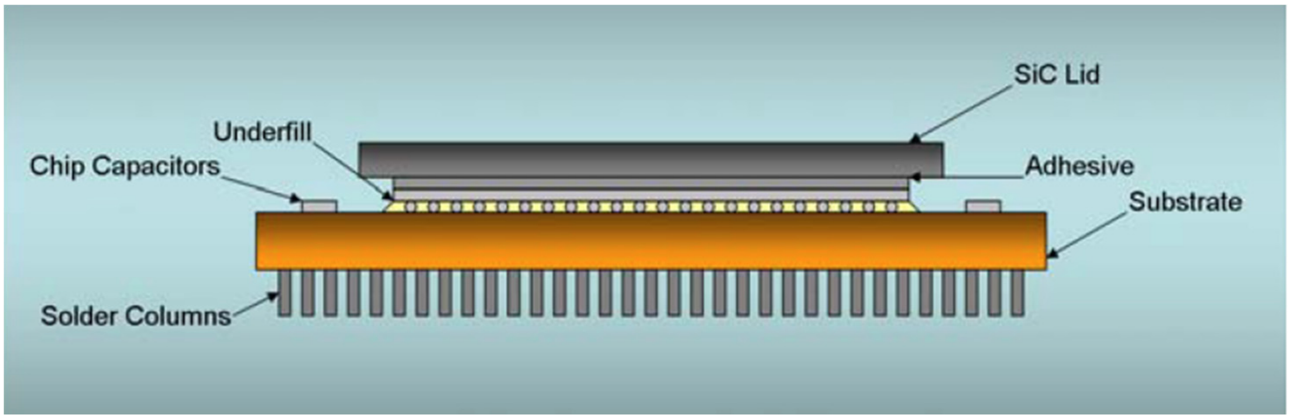


Schematic construction of a solder bump



SnAg microbump (20 µm diameter)

Xilinx V4/V5 Ceramic Package



- Each one of the highlighted areas is a qualification concern:
  - Underfill/Chip Capacitors/SiC Lid/Adhesive/Solder columns/Substrate
- Main stress tools are:
  - Temperature cycle
  - Temperature + humidity stress
  - Mechanical bond stress
- Evaluation tools:
  - C-SAM
  - Electrical test (custom and product)

FPGA Packaging – Xilinx V4 Nonhermetic

Xilinx ADQ0007

- Review and critique
- Integrate in mission requirements

Class Y

- NEPAG
- Support documentation

Physics of Failure

- Additional testing
- Overall integration and risk management

Testing on Xilinx V4/V5 Non-hermetic Package

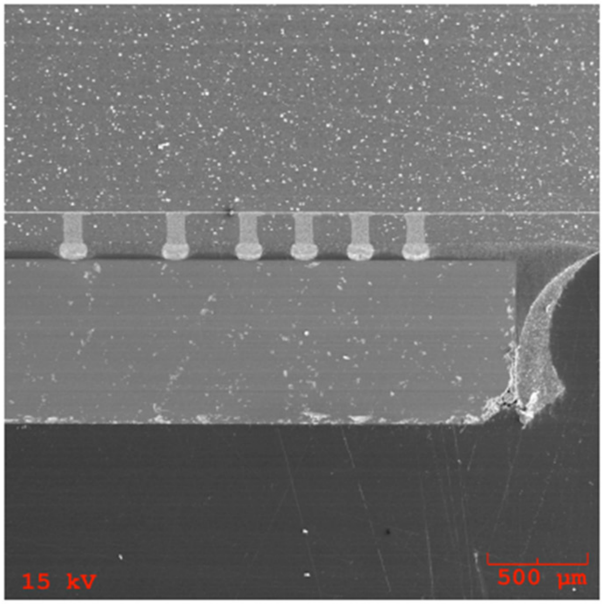
Qualification Test	Test Method	Sample Size	Device	Results
Group A testing	Mil Std 883, TM5005	100%	All 4 V4 XQR CF's	Pass
Modified* Group B Testing	Mil Std 883	per Mil Std 883	All 4 V4 XQR CF's	Pass, see Section 1
Group C testing	Mil Std 883, TM1005	15 units per device	XQR4VFX60, XQR4VLX200 & XQR4VSX55	Pass, see Section 2
Group D testing	Mil Std 883	per Mil Std 883	XQR4VLX200 & XQR4VSX55	Pass, see Section 1
Group E testing	Mil Std 883	per Mil Std 883	All 4 V4 XQR CF's	Pass
BLR Temperature Cycle Testing	IPC 9701	per IPC 9701	XQR4VLX200-CF1509	Pass, see Section 3
MLS 1 testing + CSAM	JEDEC Std 020A	15 units	XQR4VLX200-CF1509	Pass, see Section 4
Package Temperature Cycle Condition B Testing + CSAM	JEDEC & Xilinx Std	14 units	XQR4VLX200-CF1509	Pass, see Section 4
Outgassing Testing	ASTM E-595	3 units	CF Underfill and Lid Adhesive	Pass, see Section 5
Wear Out Tests	Xilinx Std	Xilinx Std	V4	Pass, see Section 6
Mask Qualification (Latch Up and ESD)	Xilinx Std	Xilinx Std	All 4 V4 XQR CF's	Pass, see Section 6

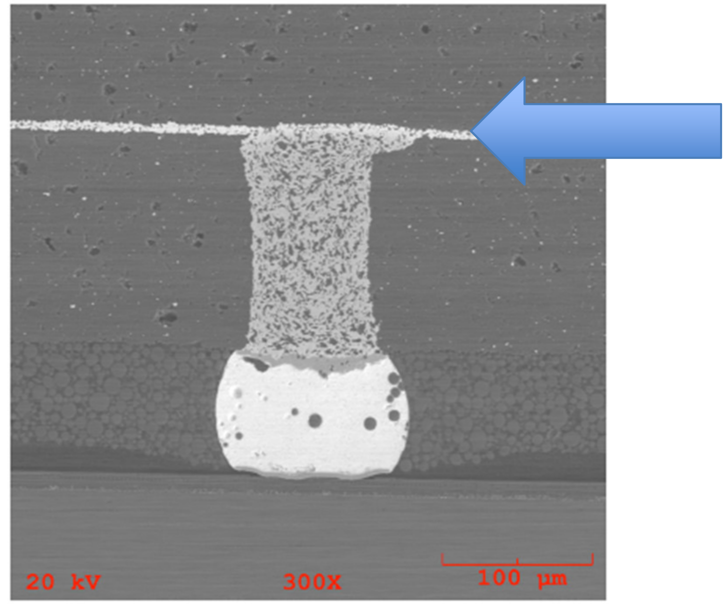
* Some tests do not apply to ceramic flip chip

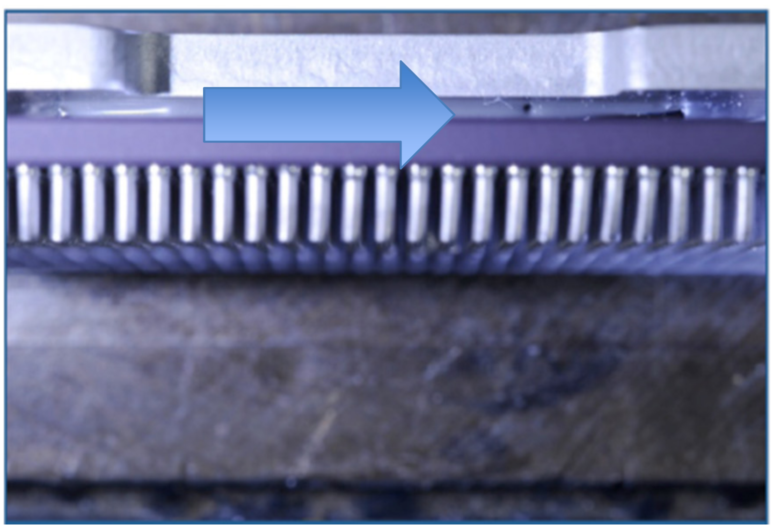
J. Fabula, "A Review of the CF Package & the Implications of addendum Y", MRQW 2010

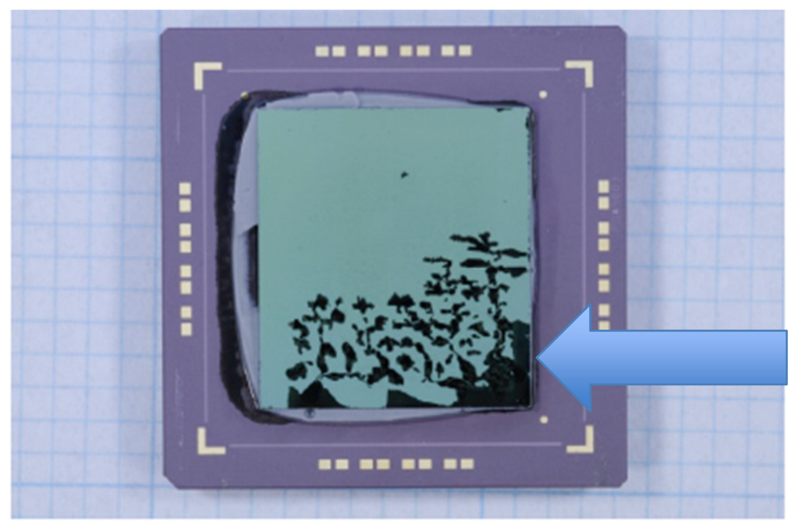
- Additional testing
  - Joint Xilinx/Customer Daisy Chain CF1752 qual
  - NEPP
    - CF1509 based board tests
    - PEM upscreening comparison of COTS FF series devices
    - Underlayer LP2 underfill – (Jong-ook Suh)
      - Thermal effects, outgassing, ageing due to plasma/radiation, vacuum, absorption.

V4 Daisy Chain – DPA

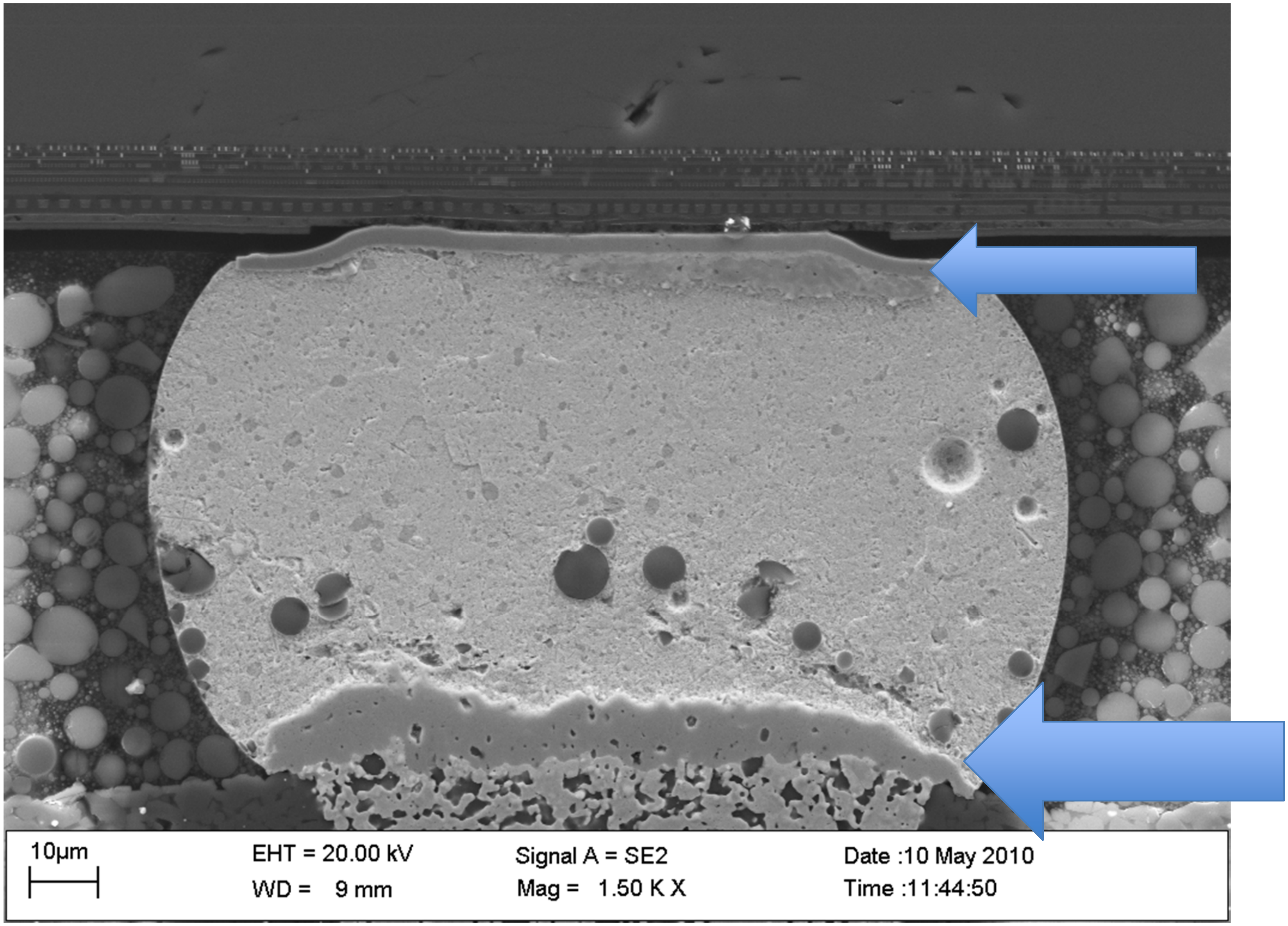




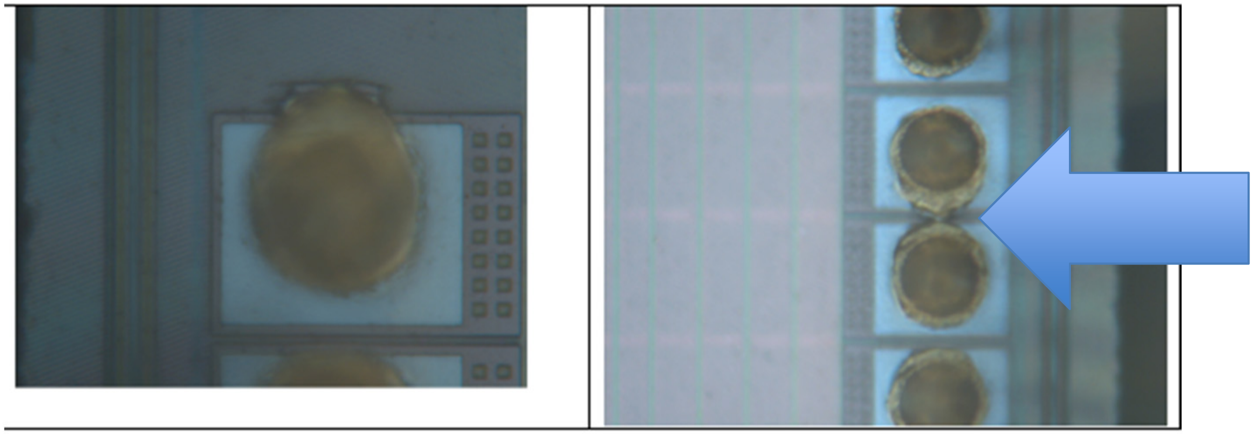


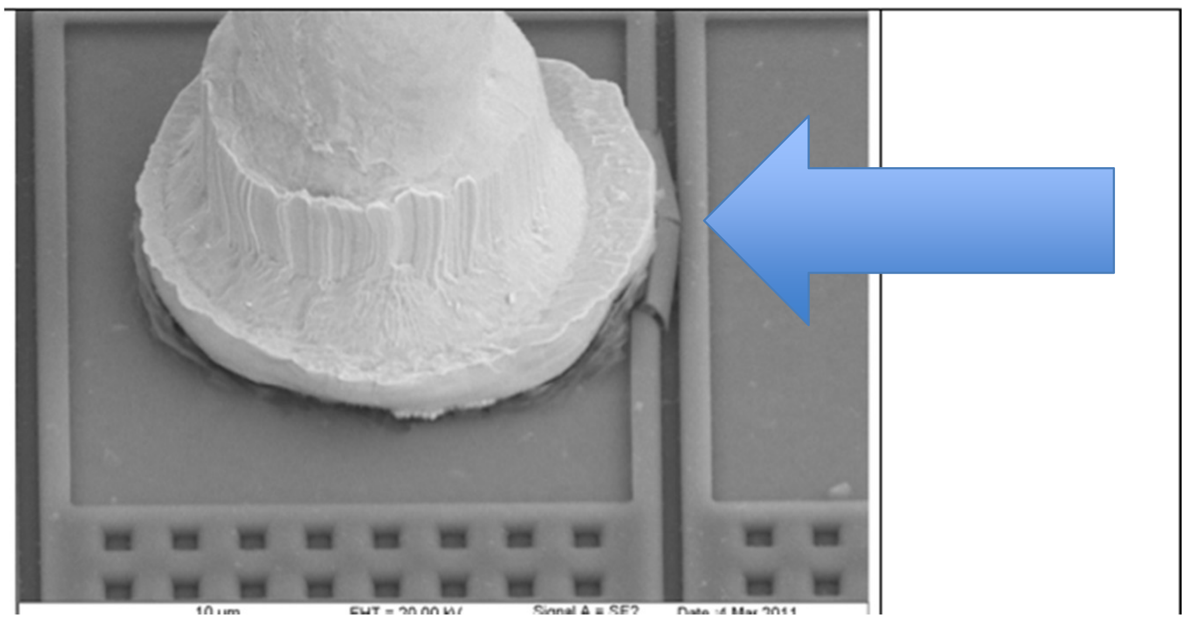


Cross Section of V4

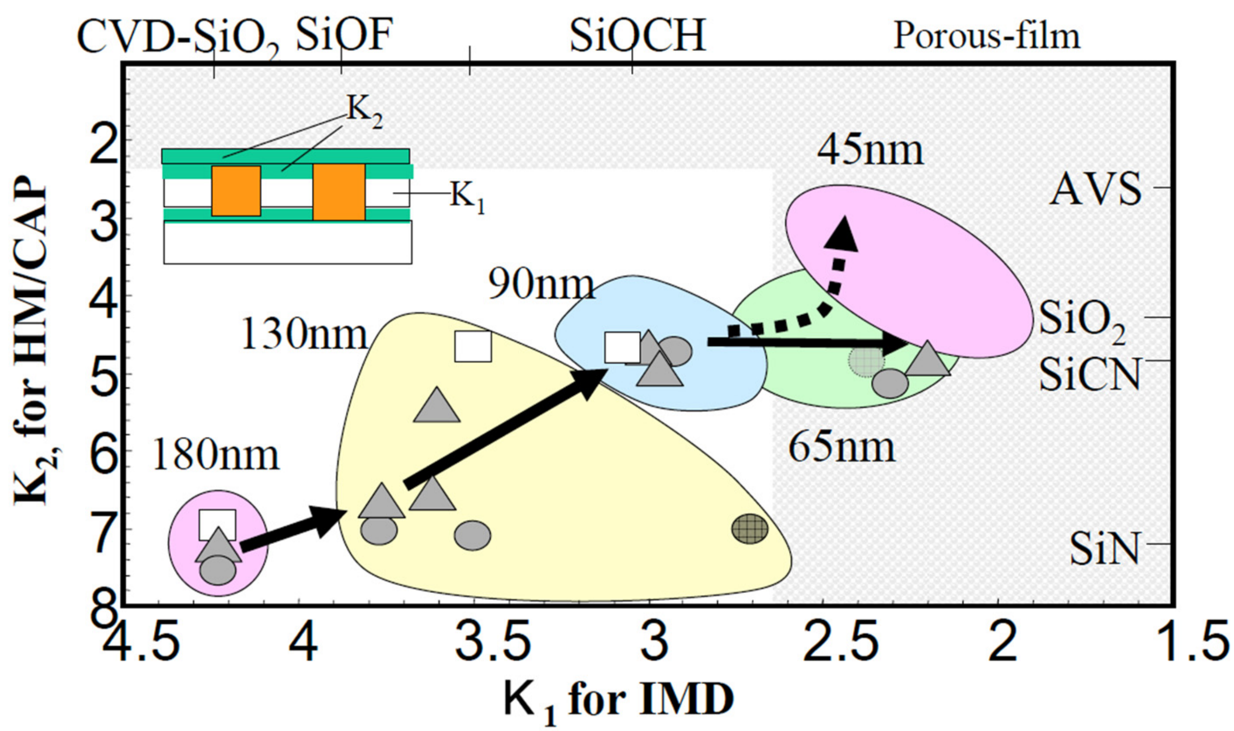


COTS Flash FPGA DPA





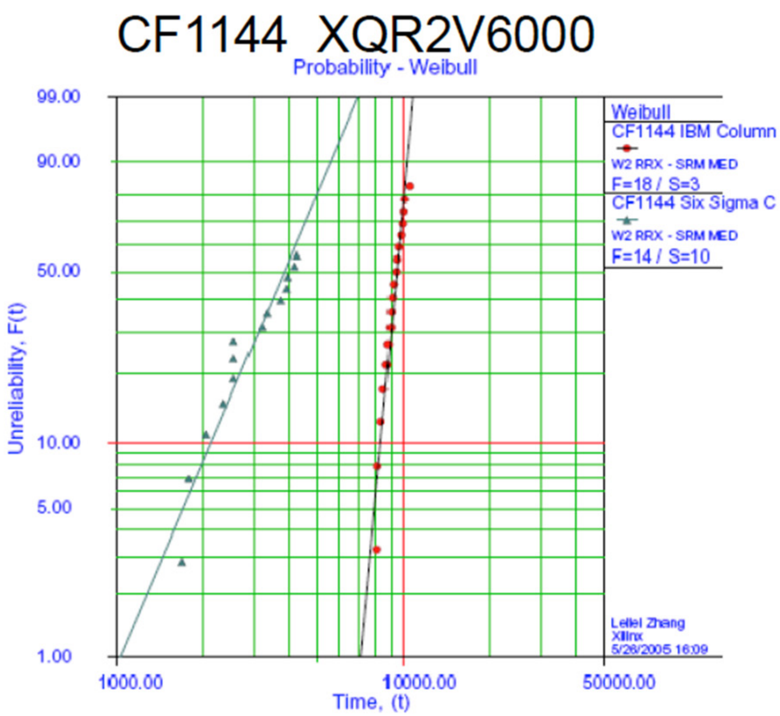
Example Technology – Packaging Interaction

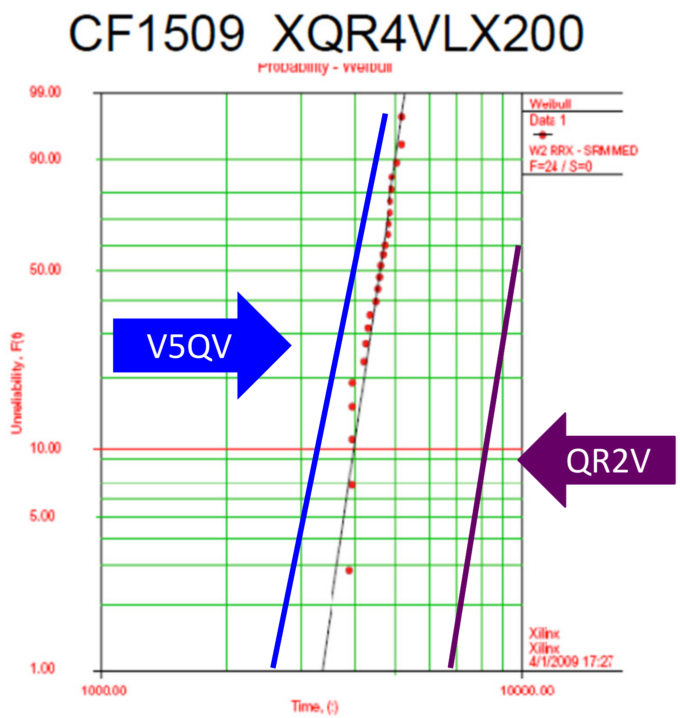


Y. Hayashi, NEC

- Scaling FPGA requires continued innovation in ILD layers
- Each of these new ILD layers has its own dielectric reliability issues PLUS interaction with overall package reliability

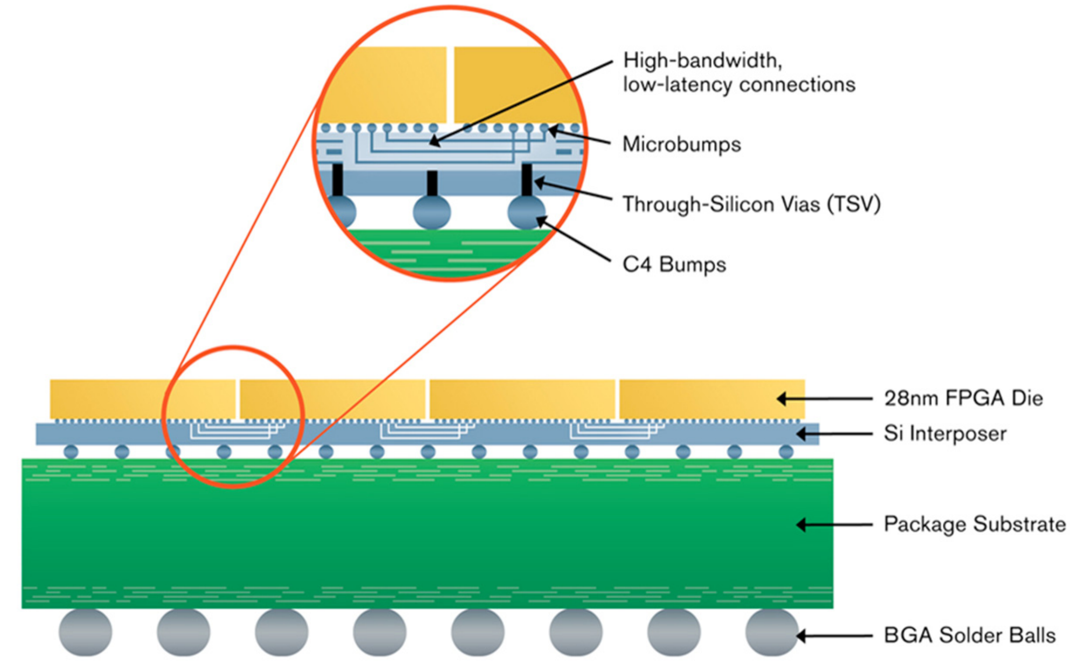
Temp cycle failures: V2 vs. V4 vs. V5





Bigger die and bigger packages have less capability in terms of total number of temp cycles (~2X)

Package – Future Challenges



- High performance FPGA to FPGA connection challenge amount of available I/O and signal latency.
- Multiple FPGA die to be combined into single package with Through-Silicon Via technology
- Provides 100x improvement/increase in inter-die bandwidth per watt over conventional approaches

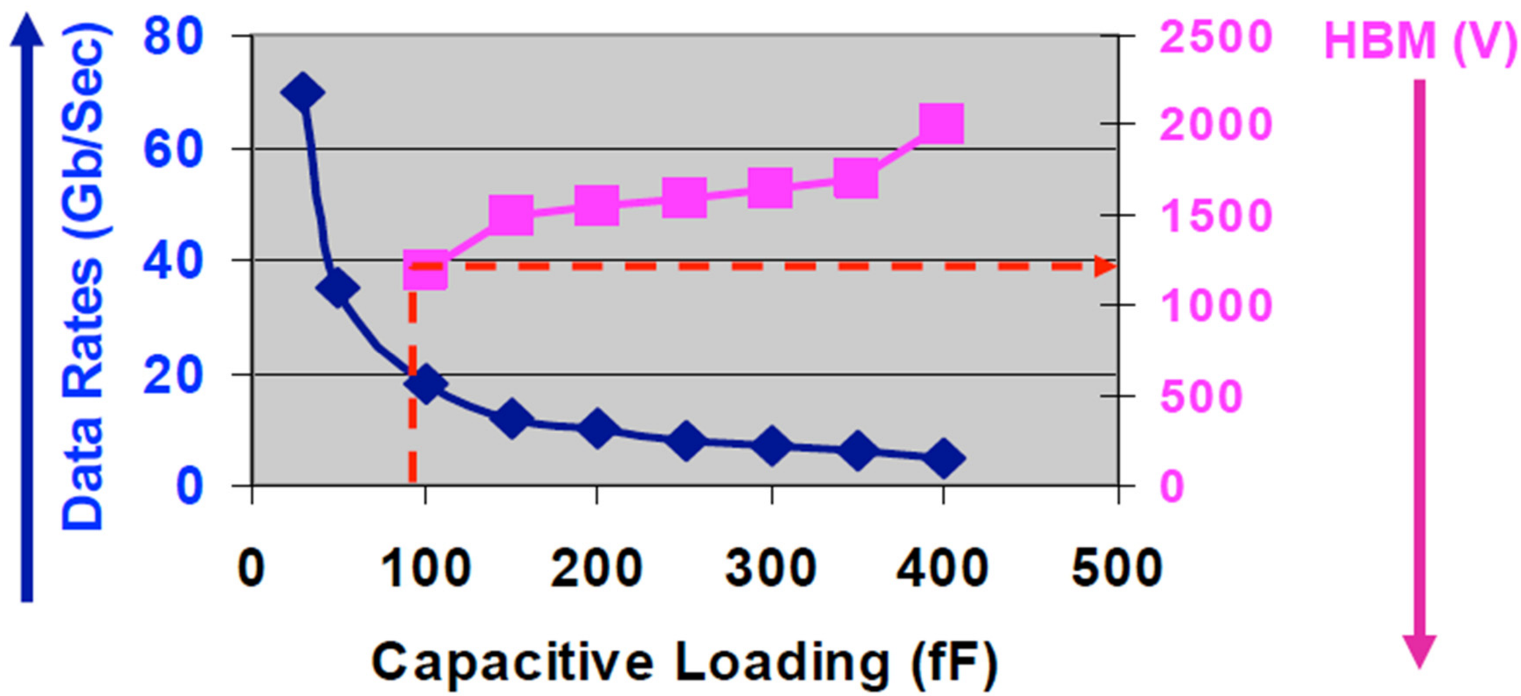
http://www.xilinx.com/technology/roadmap/ssi-technology.htm

Applications

NEPP Focused FPGA Application Assurance Support for Flight Projects

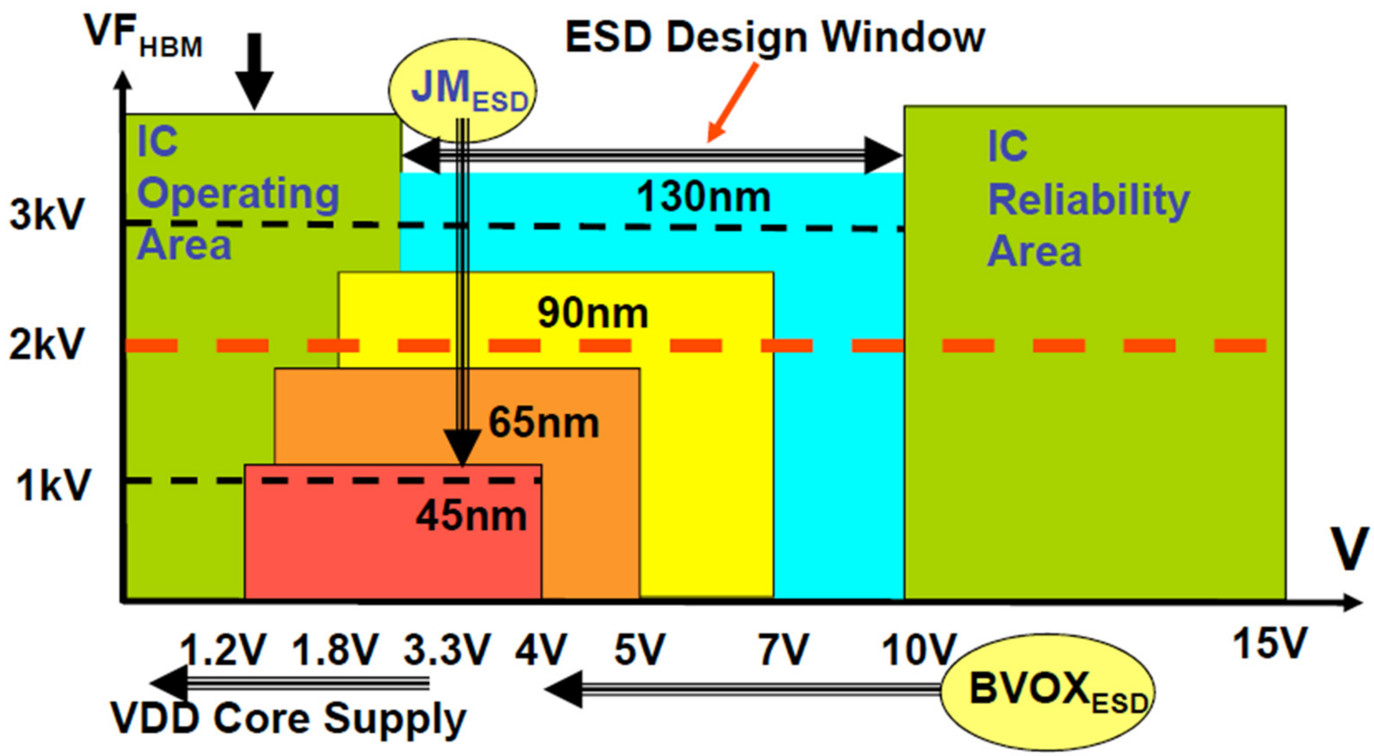
- "I did ______ to the FPGA. Is it going to be ok?"
- Provide NEPP generated engineering resource database of tests, measurements, and guidelines to support analysis:
  - Lifetime calculations based on physics of failure
  - Accelerated life test
  - Materials analysis and DPA
  - Risk management using guidelines and procedures
- Help to define next generation NEPP tasks that have broad agency relevance.
  - Materials degradations
  - SW/HW interactions
  - Technology characterization
  - Radiation Issues

Example Technology-Application Interaction: ESD influence on High Speed Designs



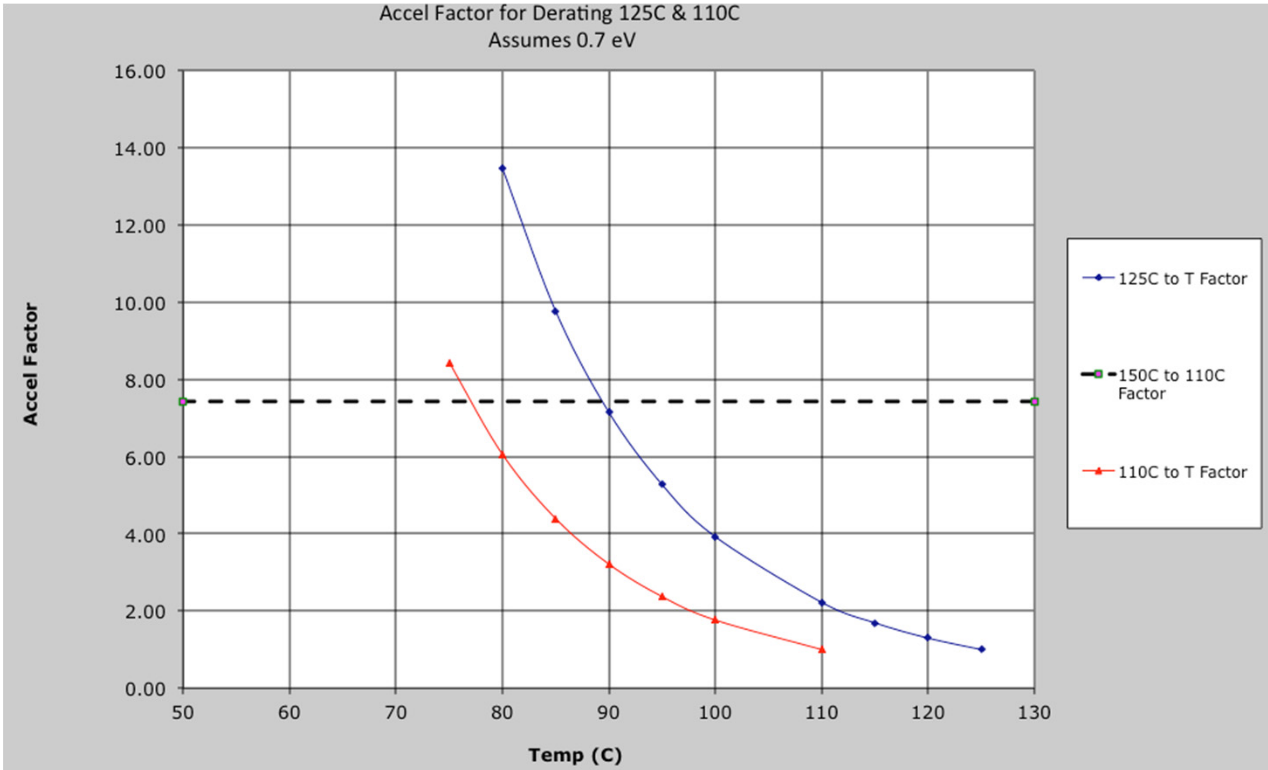
- Data Rates are influenced by the ESD loading capacitance
- The requirement of low capacitance in turn degrades ESD levels
- At 100 fF and below, 2kV HBM cannot be achieved

ESD and Technology Scaling



- Continued technology scaling results in both metal current density and oxide breakdown voltage reduction
- Result is to close the ESD Window (Vbd – Vop) for High Speed Designs making it difficult to maintain 2kV HBM

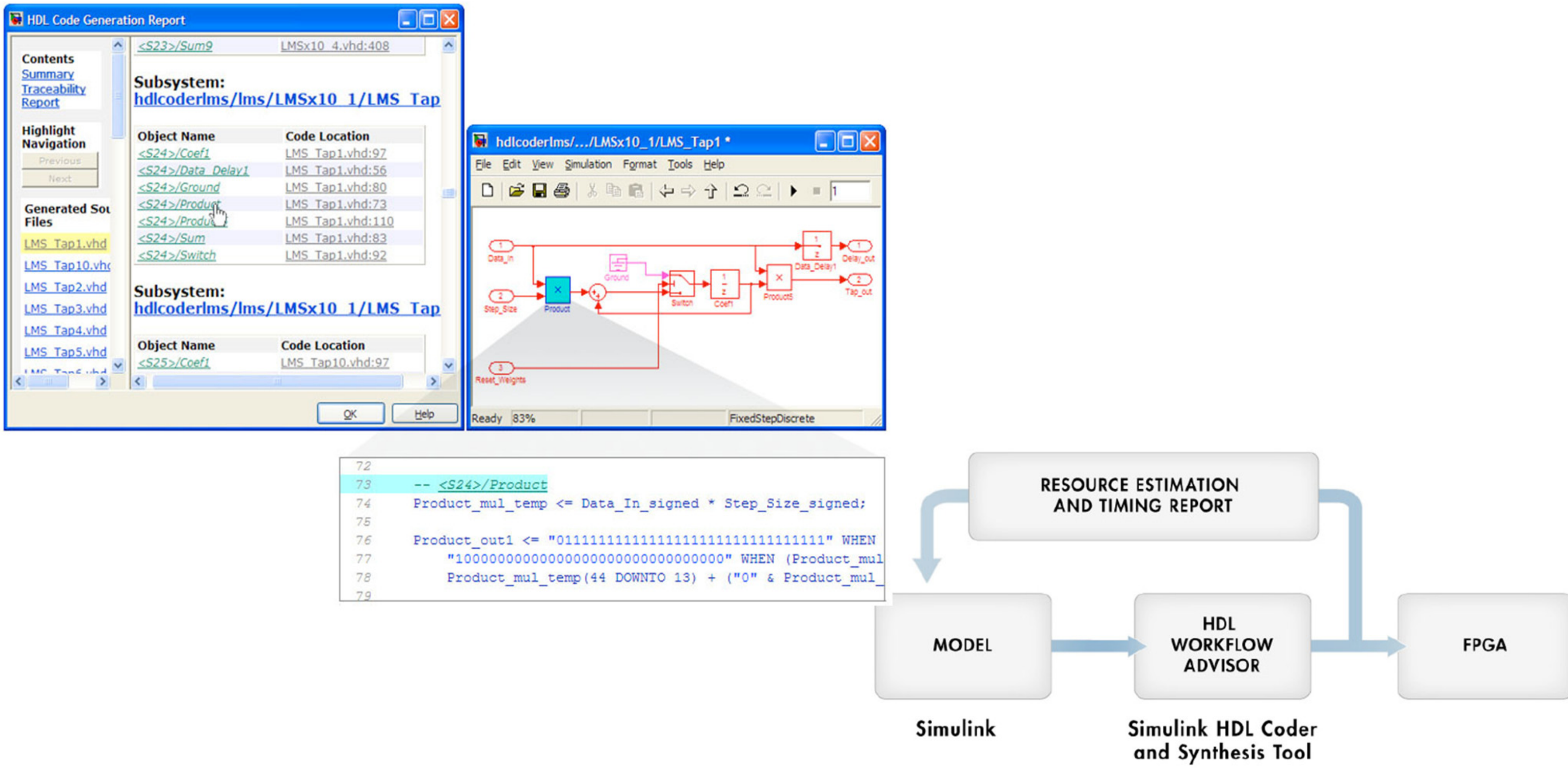
Methodology for Derating VLSI Devices



- Historically space community derated 40°C from (usually assumed) maximum of 150°C, or 110°C derated.
- Assuming 0.7eV activation energy, *the 40°C from 150°C to 110°C gives an acceleration factor of 7.43*.
  - This factor can be viewed as "margin" for long life reliability.
- Modern FPGAs have Tj_max = 125°C.
- Now we need to find what temperature gives same margin value using 125C as the new derated maximum temperature.

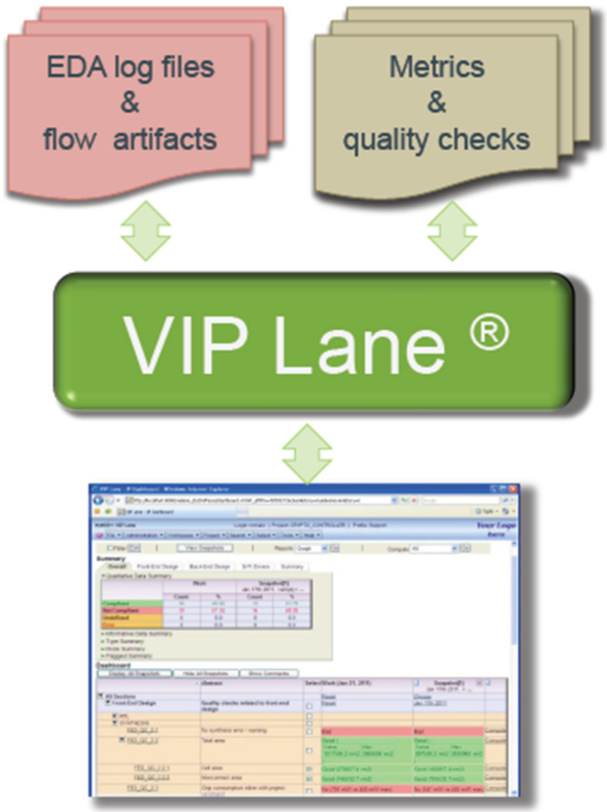
Software

Model based SW development

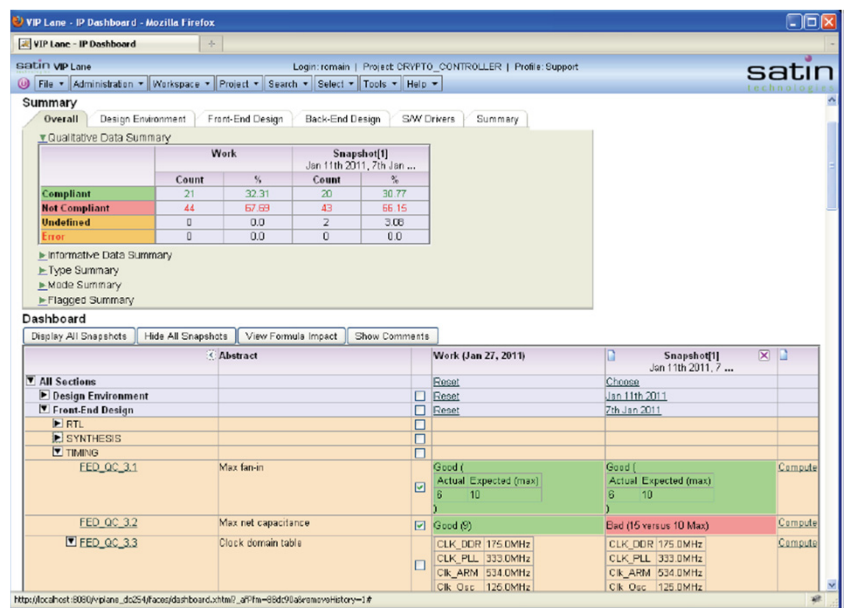


- Variety of new tools to support design validation and verification.
- DO-254 Tools and requirements
- The interaction of HW and SW

Explore Project Quality Management S/W – Satin Technologies



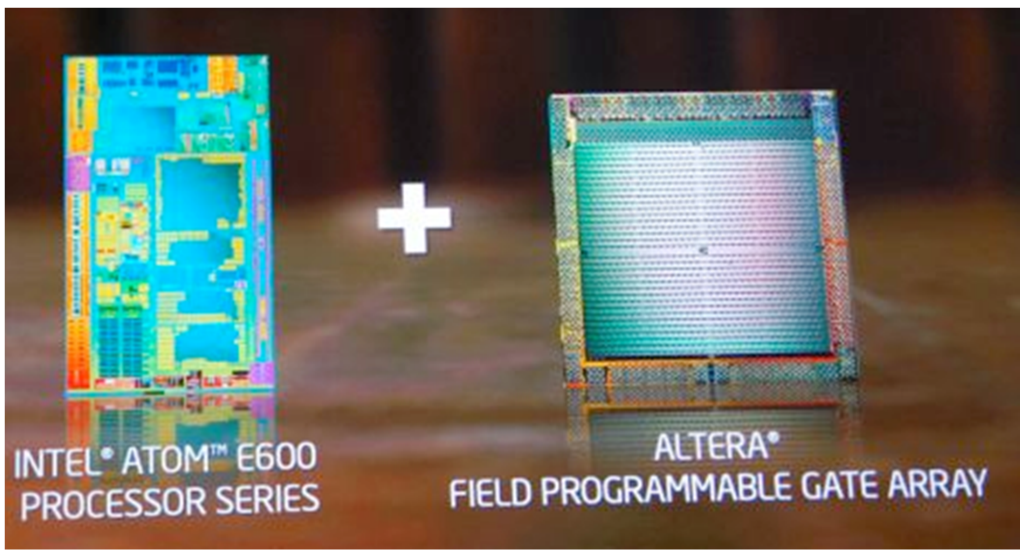
- Ability to read and analyze a wide variety of files (csv, xls, SQL, DFT and STA reports, etc.)
- JavaScript based decision and parsing formulism.
- Includes arithmetic and natural language manipulation.



The Future…

The future of commercial FPGA applications

- Intel Stellarton = Atom processor SoC + Altera FPGA
  - Emphasis on re-programmability, HW acceleration and customization
  - Xilinx V7 = FPGA + ARM microcontroller/processor
  - Actel Fusion = FPGA + ARM Cortex microprocessor
- In the future, SoC made up of processors and FPGA fabric could be standard high performance solution.



Future Direction

- FPGA use will continue in all aspects of spacecraft electronics.
- Power management will drive FPGA reliability.
  - Evolutionary improvements in on board and external measurement and better power calculators will be required to help management.
- Transition to reprogrammable FPGAs as the norm.
  - Guidelines for single event mitigation (SRAM and Flash)
- Technology reliability will require more details from foundries.
  - New materials require wafer level reliability evaluation
  - Practical life test experiments are becoming too expensive.
- Application support and IP verification may be new NEPP product.
  - Formal centers of FPGA test (HW and SW) may be required
- High Performance FPGA to FPGA systems will turn to innovative packaging schemes
  - Packaging technology & qualification will remain a key NEPP activity.